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CMOS Image Sensors and the Quanta Image Sensor

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***Abstract*—This paper briefly reviews CMOS image sensor invention and development. The focus of the paper is on a possible successor - the Quanta Image Sensor – a photon-counting image sensor that operates at room temperature without avalanche multiplication. Experimental results with 1Mpixel array devices are described.**

***Keywords*—CMOS image sensor, CIS, Quanta Image Sensor, QIS, photon-counting image sensor, single photon detector**

I. INTRODUCTION

The CMOS active-pixel image sensor with intra-pixel charge transfer “camera-on-a-chip” (CIS) was invented at the NASA Jet Propulsion Laboratory (Caltech) in 1992-1993 and further developed at JPL and then the JPL-spinoff Photobit starting in 1995 [1-3]. The low-power consumption, high-level of integration (compared to charge-coupled devices, CCDs) led to its use in new applications such as the swallowable pill-camera, and camera-phone. Further improvements by many companies around the world has led to nearly ubiquitous use of this technology for image capture in webcams, automobiles, digital still cameras and many other applications. About 5.5B CMOS image sensors were projected to be shipped in 2018 [4]. The CMOS image sensor typically uses the pinned-photodiode device in the pixel to achieve complete intra-pixel charge transfer (enabling low read noise through correlated double-sampling, for example), low dark current, and high quantum efficiency [5]. Electronic read noise is typically between 1.5-3e- rms in commercial devices, with full-well capacity of several thousand electrons.

In 2005 a new image capture concept was introduced, now called the Quanta Image Sensor (QIS). The QIS is described in a review paper [6]. In the QIS concept, the highly-specialized binary pixel is called a jot, and requires sufficient sensitivity to a single photon (or photo-electron) so that the resultant bit-error rate (BER) is sufficiently low (<0.01). The BER is directly related to the input-referred read noise. Recently, our group at Dartmouth has demonstrated excellent single-photoelectron sensitivity without the use of avalanche multiplication. We achieved deep sub-electron read noise (DSERN) below 0.2e- rms at room temperature with low dark count rate in a megapixel array [7]. A start-up company, Gigajot Technology, has been formed to further explore and develop the QIS device as a platform technology to enable a number of photon-counting image sensor applications.

II. JOTS IN MODIFIED CIS FABRICATION PROCESSES

A. *Avoiding Avalanche Multiplication*

For photon-counting with very fast time resolution, it is hard to beat the single-photon avalanche detector (SPAD) which uses avalanche multiplication to achieve signal gain. However, to date such pixels are relatively large (e.g. 5-20um pitch) due to the high electric fields and the concomitant isolation required between pixels. Further, the high electric field can result in high dark count rates (e.g. 100-5,000 counts/s/pixel) and low manufacturing yield, further limiting achievable and economical array sizes. Resolution of photon number is also a challenge when using avalanche multiplication, such as in electron-multiplying CCDs (EMCCDs). For these reasons, we wished to achieve gain without using avalanche multiplication.

B. *Tiny Sense Node Capacitance for High Conversion Gain*

An alternative approach to gain is to use a tiny sense node capacitance. In CIS devices, photo-generated charge is integrated and then transferred to a sense-node. The change in voltage on the sense node is proportional to the charge and inversely proportional to the capacitance. For example, if the sense node capacitance was 0.16fF, then a single electron’s charge would correspond to a change in sense node voltage of 1mV, typically well above the noise floor of the in-pixel buffer amplifier (source-follower). Thus, an early aim of our research was to reduce the sense node capacitance. Typical conversion gains (electron charge divided by capacitance) that have been achieved are 300-400uV/e- and improvement is still underway. Essentially one must eliminate overlap and stray capacitances from the sense node. We used a “pump-gate” approach and different reset structures to achieve this, requiring some implant changes but no new masks in the standard CIS process.

C. *Backside-Illuminated (BSI) Pump-Gate Jot Structure*

The structure of the jot and its operation have been described in [6,7] and is illustrated in Fig. 1. Photons enter the “backside” of the device. Photoelectrons are generated in the silicon and are collected and integrated in the storage well (SW). At the time of read out, the sense node (FD) is reset to a high voltage (e.g., 2.8V) using a reset device not shown. The transfer gate (TG) is then pulsed high, pulling the photoelectron(s) to the surface. The TG is then returned to low voltage (e.g., 0V). Due to the electric-field shaping caused by

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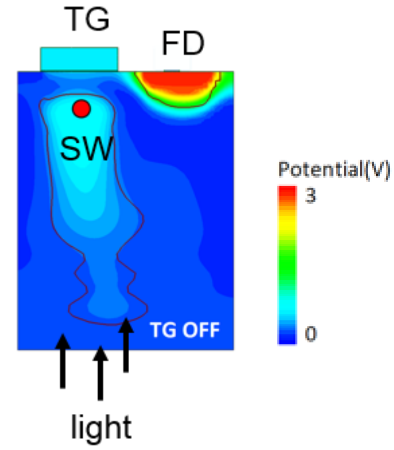

Fig. 1. Cross-section of QIS jot, with color-coded electrostatic potential and photoelectron shown as red dot.

implant profiles, the photoelectron is "pumped" to FD causing a change in FD voltage. The SW has a capacity to store a hundred or so electrons in the current device.

To sense the change in FD voltage, the FD is connected to an in-pixel buffer amplifier (e.g., MOSFET or JFET source-follower). The voltage change on FD is read out using correlated double sampling (CDS) or correlated multiple sampling (CMS) techniques. Due to downstream noise, we found some small improvement with CMS over the standard CDS method in the case of analog readout of the sensor.

Generally, the readout noise is limited by residual noise from the in-pixel buffer-amplifier transistor, manifested as 1/f or random telegraph signal noise, and the noise of each pixel varies, probably due to different traps and scattering centers.

D. Experimental Results

An example photon-counting histogram (PCH) is shown in Fig. 2 and clearly shows photoelectron quantization. The horizontal axis is readout voltage, which has been normalized

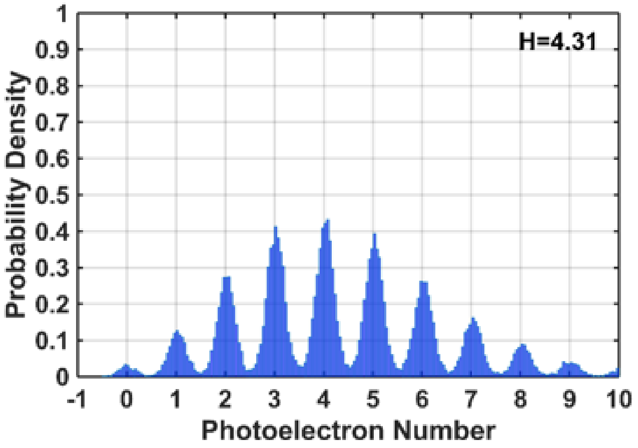

Fig. 2. Photon-counting histogram (PCH) from a single pixel, 20,000 reads, each read uisng 20CMS cycles, at room temperature.

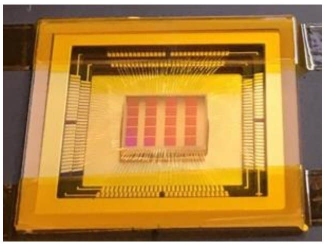

Fig 3. Twenty (20) different 1Mpixel QIS arrays, half digital readout, half analog readout.

by the conversion gain of 350uV/e-. From the PCH we can determine the input-referred read noise of 0.175e- rms corresponding to a BER of approx. 0.002 errors/read. The average photo-electron number is 4.31e- as determined from the relative peak heights, which follow a Poisson distribution. Input-referred read noise was found to reduce a bit at lower temperature. No significant lag was found and dark current was below 0.2e-/s at room temperature.

Twenty different 1Mpixel sensor designs have been fabricated in the TSMC BSI stacked CIS process, all on the same chip, as shown in Fig. 3. The digital-output arrays operate up to 1000fps and each array dissipates less than 20mW due to the cluster-parallel readout architecture and low-power-readout circuit design. Details can be found in [7] along with an example 1Mpixel photon-counting image taken with the QIS.

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REFERENCES

[1] e.g., US Patent 5,471,515 and US Patent 5,841,126

[2] E.R. Fossum, "Camera-on-a-Chip: Technology Transfer From Saturn to Your Cell Phone," Technology and Innovation, Vol. 15, pp. 197–209, December 2013. https://doi.org/10.3727/194982413X13790020921744

[3] NASA Spinoff 2017 retrieved from: https://spinoff.nasa.gov/Spinoff2017/toc_2017.html 5-July-2018.

[4] Retrieved from: http://www.icinsights.com/news/bulletins/Nonstop-CMOS-Image-Sensor-Sales-Records-Seen-Through-2021/ 5-July-2018.

[5] E.R. Fossum and D. Hondongwa, "A review of the pinned photodiode for CCD and CMOS image sensors," IEEE J. Electron Devices Society, vol. 2(3) pp. 33-43 May 2014. doi: 10.1109/JEDS.2014.2306412

[6] E.R. Fossum, J. Ma, S. Masoodian, L. Anzagira, and R. Zizza, "The quanta image sensor: every photon counts," MDPI Sensors, vol. 16, no. 8, 1260; August 2016. (Special Issue on Photon-Counting Image Sensors) https://doi.org/10.3390/s16081260

[7] J. Ma, S. Masoodian, D. Starkey, E.R. Fossum, "Photon-number-resolving megapixel image sensor at room temperature without avalanche gain," OSA Optica, vol. 4, no. 12, pp.1474-1481, December 2017. https://doi.org/10.1364/OPTICA.4.001474

[8] D. Starkey, W. Deng, J. Ma, S. Masoodian, E. R. Fossum, "Quanta imaging sensors: achieving single-photon counting without avalanche gain," (keynote) in Proc. SPIE 10639, Micro- and Nanotechnology Sensors, Systems, and Applications X, 106391Q Orlando Florida USA, April 18, 2018; doi: 10.1117/12.2309630