Room Temperature 1040fps, 1 Megapixel Photon-Counting Image Sensor with 1.1um Pixel Pitch

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ABSTRACT

A 1Mjot single-bit quanta image sensor (QIS) implemented in a stacked backside-illuminated (BSI) process is presented. This is the first work to report a megapixel photon-counting CMOS-type image sensor to the best of our knowledge. A QIS with 1.1µm pitch tapered-pump-gate jots is implemented with cluster-parallel readout, where each cluster of jots is associated with its own dedicated readout electronics stacked under the cluster. Power dissipation is reduced with this cluster readout because of the reduced column bus parasitic capacitance, which is important for the development of 1Gjot arrays. The QIS functions at 1040fps with binary readout and dissipates only 17.6mW, including I/O pads. The readout signal chain uses a fully differential charge-transfer amplifier (CTA) gain stage before a 1b-ADC to achieve an energy/bit FOM of 16.1pJ/b and 6.9pJ/b for the whole sensor and gain stage+ADC, respectively. Analog outputs with on-chip gain are implemented for pixel characterization purposes.

Keywords: Photon counting detector, quanta image sensor, QIS, CMOS image sensor, CIS, charge-transfer amplifier

1. INTRODUCTION

The quanta image sensor (QIS) was introduced in 2005 as a paradigm shift in image capturing to take advantage of shrinking pixel sizes enabled by technological advancements [1]. The QIS contains a large number of sub-diffraction-limit, high-conversion-gain, low-full-well-capacity pixels, called "jots." The key aspects of the QIS involve counting individual photoelectrons using the jots at high readout rates, representing this binary output as a bit cube (x,y,t), and finally, processing the bit cubes to form high dynamic range images [2]. The QIS concept is illustrated in Figure 1.

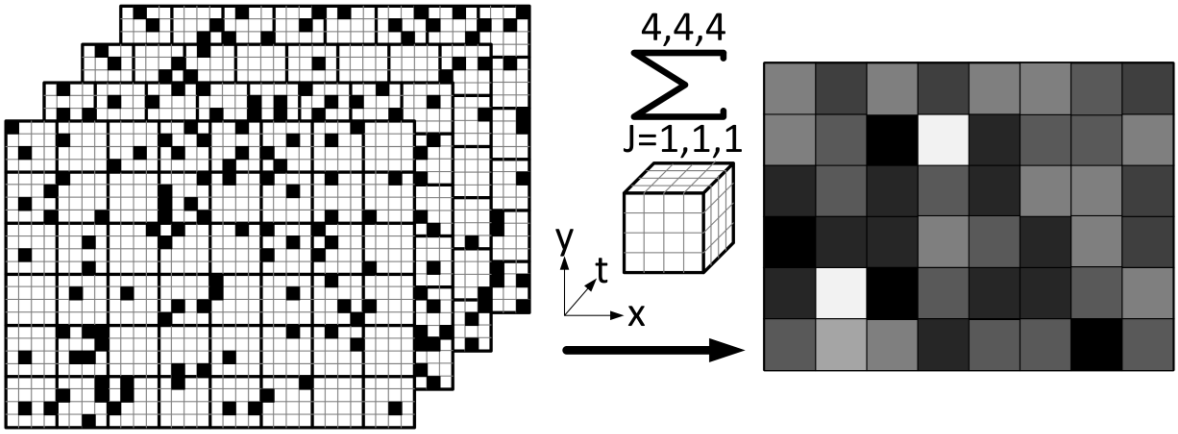

Figure 1. QIS concept. Every solid square in each temporal field represents a photo-electron created by absorbing a photon. A cubicle of jots, consists of spatial and temporal jots and forms each output image pixel. In this illustration, a 4x4x4 jot cubicle is used. In a QIS system, the cubicle size is a parameter in the image formation processing that occurs post capture.

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A QIS may contain over a billion jots, each producing just a small amount of signal per electron conversion, with a field readout rate 10-100 times faster than conventional CMOS image sensors.

The two biggest challenges in designing a high-field-readout rate gigajot QIS are realizing the jots (tiny, single-photon detector) and the high-speed, low-power readout circuits. Several prior works have been published from our research group to address these challenges and develop solutions for the jot device as well as high-speed, low-power readout circuits. Most of these works are covered in [2].

The read noise of an image sensor determines its photoelectron counting capability. Deep sub-electron read noise (DSERN) is required for photoelectron counting, corresponding to an input-referred read noise of 0.5e- r.m.s. or lower. To realize accurate photoelectron counting with minimal counting error rate, read noise less than 0.15e- r.m.s. is ultimately desired for QIS applications. In QIS-type readout circuitry, the in-jot source follower (SF) is the major contributor of read noise. Approaches for eliminating QIS read noise include enhancing the conversion gain (CG) on the floating diffusion (FD) node and reducing the voltage noise from the SF.

The pump-gate jot with tapered reset (TPG) was proposed by our group to enhance the CG of jots to the range of 400μV/e-. In 2015, read noise of 0.22e- r.m.s. (in the best jot device) was demonstrated in a small 32x32 test array, and was the first time the photoelectron counting capability was demonstrated without using avalanche multiplication gain at room temperature [2]. These previous results motivated us to merge the TPG jot with the QIS-type readout circuits in a more sophisticated sensor system. To achieve this goal, a prototype chip which contains 20 different 1Mjot arrays was designed and fabricated in a 65/45nm stacked BSI process. Among the 20 1Mjot arrays on this chip, in this paper the results of the array with TPG jots are reported. Also, in this paper the first practical stacked backside-illuminated (BSI) 1Mjot single-bit QIS is presented. It achieves a frame rate of at least 1040fps.

2. SENSOR

2.1 Sensor architecture

The simplified structure of the imager is shown in Figure 2. A stacked QIS uses two substrates, with the substrates being stacked vertically and electrically connected, with the photo-detectors and circuits on different substrates. The jots are implemented on the detector substrate and the readout circuits and addressing circuits are located on the ASIC substrate. Each cluster of jots is associated with its own dedicated readout electronics stacked under the cluster. Twenty (20) different 1Mjot arrays are implemented in this chip, where every array has a different variation of jot and readout design. Figure 3 shows a photograph of the QIS test chip. There were two classes of readout designs, one supporting analog readout for detailed characterization, and one supporting binary data readout at much higher field rates.

The jots are two-way shared (2(H)x1(V)) and every 4096 jots (one cluster of jots) share a 1-bit ADC (Figure 4). There are a total number of 256 1-bit ADCs for all the 256 clusters in the imager. The readout of all the clusters is performed in a parallel manner and 32 high-speed digital pads are used to send the data off-chip.

2.2 Jot device

In this paper, the results of the arrays (analog and digital) with the tapered-pump-gate (TPG) jots [3] are presented. The TPG jots are fabricated with a 45nm BSI CMOS image sensor (CIS) process. The schematic of the 2 way-shared jots is shown in Figure 4. The simplified layout of the jots is depicted in Figure 5a. As shown in Figure 5a, the pump-gate photodiode doping profile is adapted from the previously demonstrated design and optimized for an improved effective fill-factor and better response in the shorter wavelength regime.

2.3 Analog-to-digital converter

The 1-bit ADC is comprised of two cascaded charge-transfer amplifiers (CTA) followed by a dynamic latch (d-latch). Cascading two CTAs amplifies the input voltage to a level which is larger than the input-referred offset of the d-latch [4]. In comparison with [4], in this design, the stacked structure makes it possible to reduce the aspect ratio of the CTA, therefore, instead of 4 cascaded CTAs, two cascaded CTAs are used. The threshold of the ADC can be set by adjusting the Vpro in the CTA.

The 1-bit ADC is designed and fabricated with 0.25μm gate-length CMOS transistors to provide a wide input common-mode range (ICMR) to handle the wide range of jot designs. However, to reduce the power consumption of the ADCs in

future designs, smaller feature nodes such as 65nm can be used by limiting the ICMR according to a specific jot design. At 1040fps, the ADC sampling rate is about 4MSa/s and each ADC consumes 29µW.

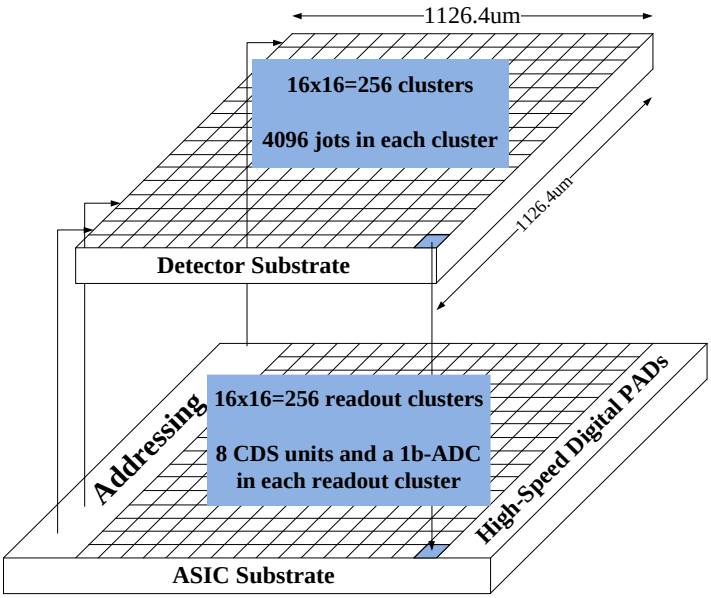

Figure 2. Simplified architecture of 1Mjot stacked QIS.

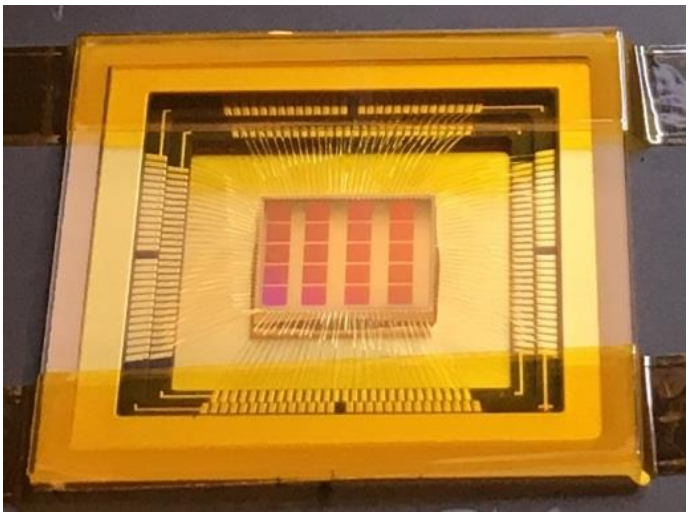

Figure 3. Photograph of the 20x1Mjot QIS test chip.

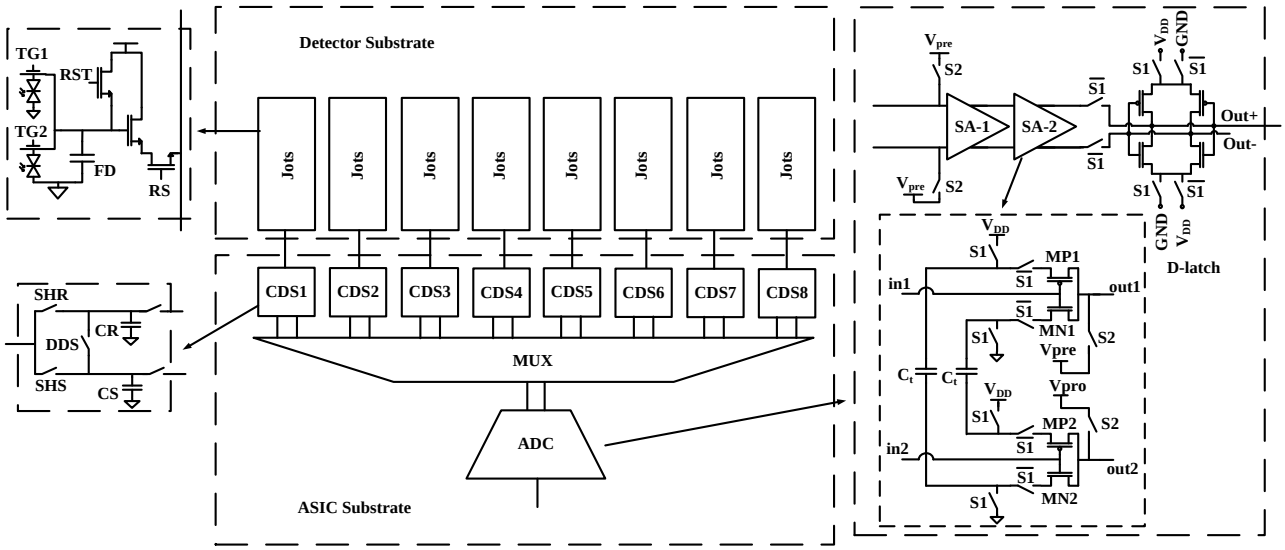

Figure 4. Schematic of a cluster of jots and a readout unit for digital output.

2.4 Sensor function

The sensor is readout using a rolling shutter with full-frame integration. After a row is selected, the jots are reset, and the voltage values of the reset levels are stored on the CR capacitor in the CDS unit. By activating the TG, the collected charge is transferred from the storage-well in the jot to the floating diffusion, and the signal values are sampled onto the CS capacitor in the CDS unit. The differential signals stored in the CDS units are applied to the input of the ADC for quantization. After quantization is completed, the outputs of the 256 ADCs are sent out off-chip via 32 high-speed pads.

3. EXPERIMENTAL RESULTS

Figure 5 shows the characterized results of the TPG jots. These results were achieved using the slower analog outputs with an on-chip gain of 10(V/V) and a 14-bit on-board ADC. The simplified schematic of the analog readout chain is shown in Figure 6. Each column output line is connected to a correlated double sampling (CDS) unit. The output of every 4 CDS units are selected by a multiplexer and sent to a unity-gain buffer. The buffered signal is then amplified by a switch capacitor programmable gain amplifier (PGA). Another unity-gain amplifier is used to drive the output pad after the PGA. For the best noise performance, correlated multiple sampling (CMS) was used to suppress the noise in the readout chain, where 20 cycles of signal were collected in series. It was found that additional cycles could not reduce the read noise, probably because of the addition of low-frequency noise due to the extended readout process.

The CG and read noise were characterized with the photon counting histogram (PCH) method. In this measurement, the PCH of each jot was created from 20k continuous reads. The read noise was extracted from the valley-peak-modulation (VPM), and the conversion gain was extracted from the peak-to-peak distance. The inevitable variability in the fabrication process always leads to performance variation between each jot. For example, small misalignment of masks may lead to variation of CG, and the randomness in the number of traps in each jot's source-follower may lead to different voltage noise magnitude. Since the analog readout speed is currently limited on the testing board, about 8192 jots of each type were tested. Figure 5b shows the photon-counting histogram (PCH) of the best jot in the array with a read noise of 0.18e-r.m.s.. Histograms of the conversion gain and read noise for the jots are shown in Figure 5c and 5d, respectively. The average conversion gain is 345μV/e- and the conversion gain variation is 2.9%. The average read noise is 0.236e-, the peak of the read noise histogram is 0.22e-, the best and worst read noise cases are 0.18 and 0.39e-r.m.s., respectively. The variation of read noise is 16%. Note that a relatively long tail was observed in the read noise distribution, and the jots with higher noise were found to have stronger high-frequency noise. Further investigation is needed to discover the source of noise, but the suspicion is interface-trap-related RTS noise.

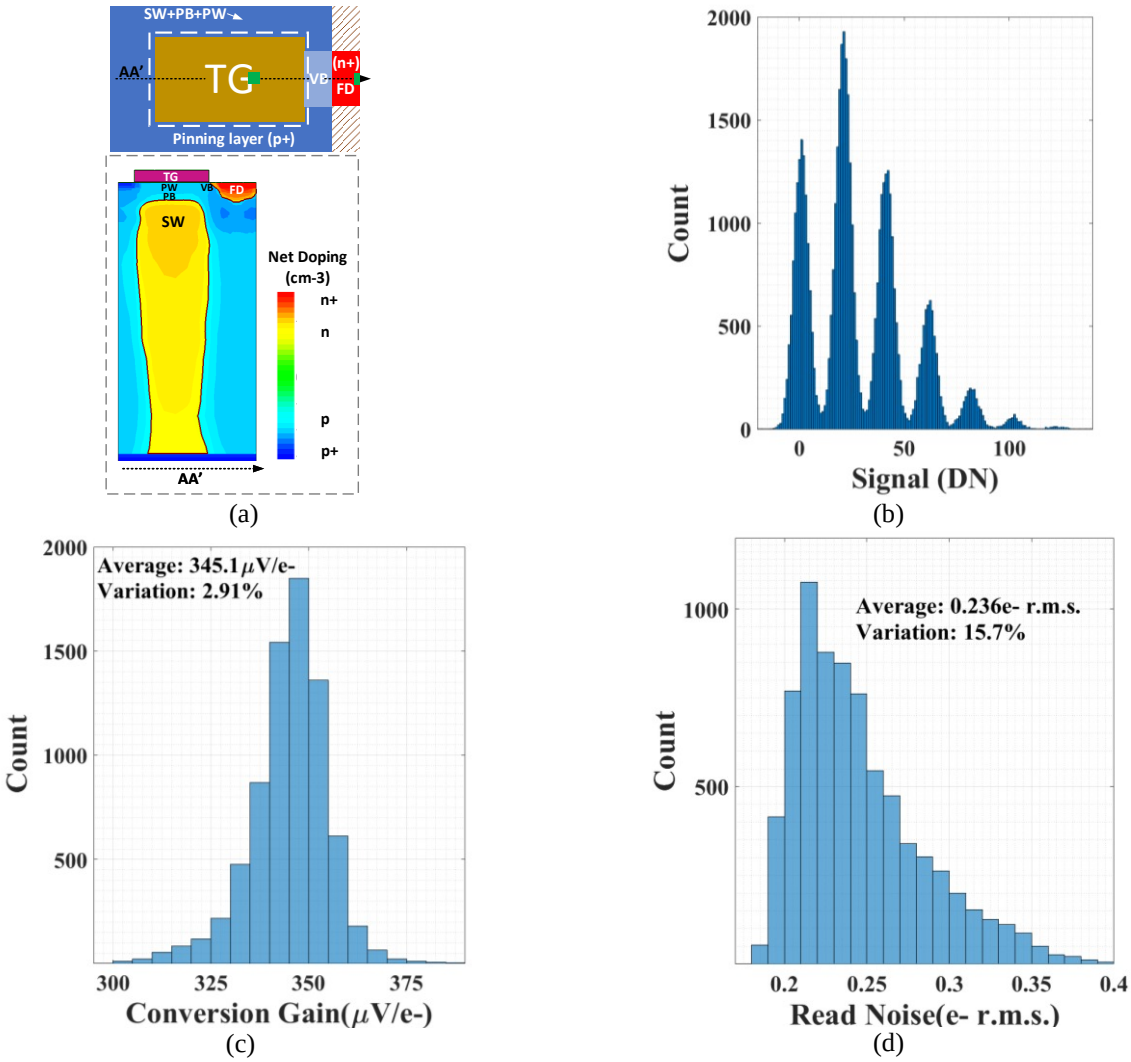

Figure 5. (a) Simplified layout and simulated doping profile of the pump-gate photodiode; (b) PCH of the golden TPG jot with 0.18e-r.m.s. read noise; (c) Conversion gain variation of the TPG jots; (d) Read noise variation of the TPG jots.

Specifications of the imager are shown in Table I. The sensor functions at 1040fps and with 1Gb/s output data rate, resulting in a total power consumption of 17.6mW. The energy-per-bit FOM is defined as:

$$FOM = \frac{power}{\#of\ pixels \times fps \times N} \quad (1)$$

where N represents the ADC resolution in bits, which for algorithmic converters is the number of comparator strobes per conversion. The 1Mjot QIS has a FOM of 16.1pJ/b (including output pads) and considering only the gain+ADC power, the FOM of the QIS becomes 6.9pJ/b. Compared to [4], even though the FOM of the ADC is increased (which we expected, because a bigger feature node is used in this design), the total FOM is reduced because the stacked architecture and cluster readout helps to reduce the needed bias current to achieve this high-speed readout. Considering only the array power, the FOM in this stacked sensor is improved more than 3 times in comparison with [4].

Examples of experimental images formed from collected QIS data are shown in figure 7.

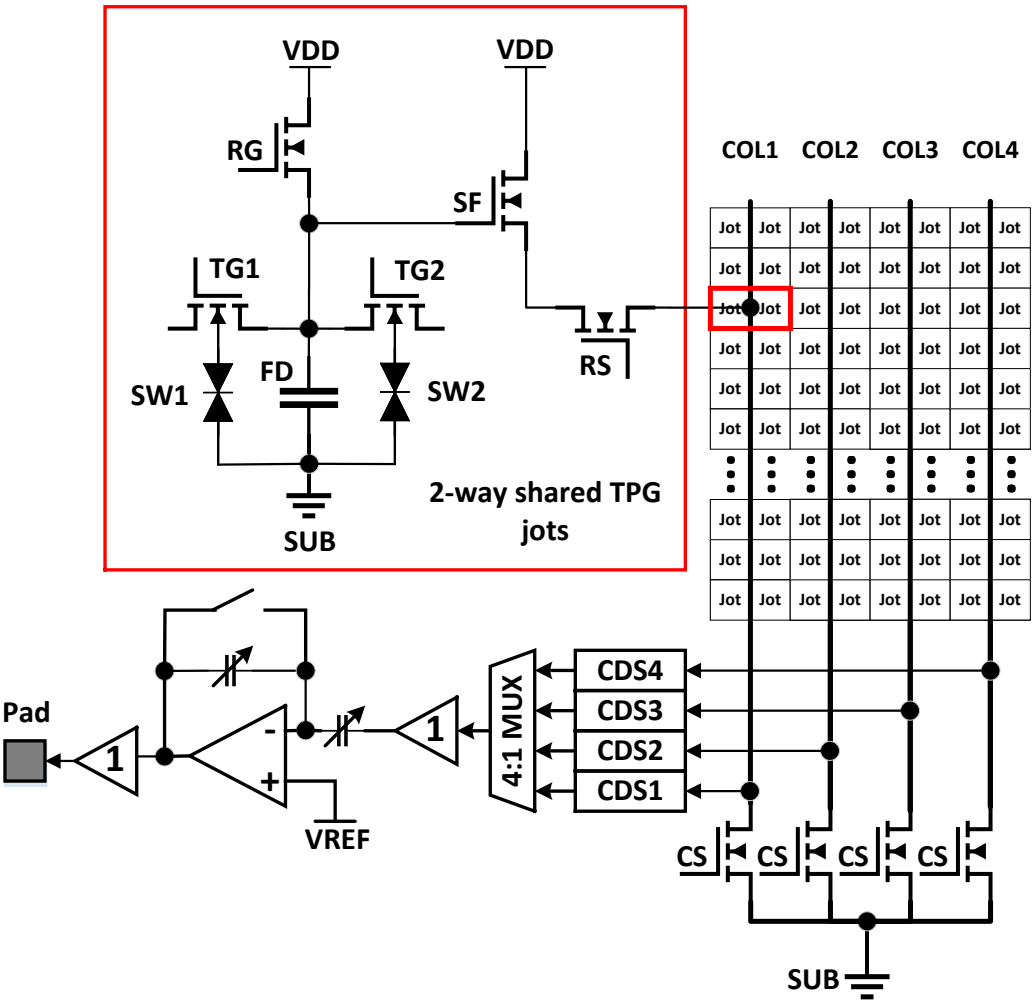

Figure 6. Simplified schematic of one on-chip readout unit for analog outputs.

Table I. Specifications of the 1Mjot single-bit QIS.

Process	45nm (jot layer), 65nm (ASIC layer)
VDD	1.8V & 2.5V (Analog, digital and array), 3V & 2.2V (I/O pads)
Jot type	BSI Tapered Pump Gate/2-Way Shared RO
Jot pitch	1.1μm
BSI Fill Factor	~100%
Quantum Efficiency	To be measured, visible band
Conversion gain on column	345μV/e-
Input Referred Noise	0.22e- r.m.s.
Corresponding BER	~1%
Avg. Dark current (RT)	0.16e-/s
Equiv. Dark Count Rate (RT)	0.16Hz/jot
Equiv. PD Dead Time	<0.1%

Array		1024 (H) x 1024 (V)
Field rate		1040fps
ADC sampling rate		4MSa/s
ADC resolution		1 bit
Output data rate		32 (output pins) x 34Mb/s = 1090Mb/s
Package		PGA with 224 pins
Power	Array	2.3mW
	256 ADCs	7.5mW
	Addressing	4.1mW
	I/O pads	3.7mW
	Total	17.6mW
FOM ADC		6.9pJ/b

4. ACKNOWLEDGMENTS

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REFERENCES

[1] Fossum, E.R., "What to do with sub-diffraction limit (SDL) pixels? - a proposal for a gigapixel digital film sensor (DFS)," in IEEE Workshop on CCDs and Adv. Image Sensors, Karuizawa, (Japan, June 2005).
[2] Fossum, E. R., Ma, J., Masoodian, S., Anzagira L. and Zizza, R., "The quanta image sensor: every photon counts," MDPI Sensors, 16(8), p. 1260, (2016).
[3] Ma, J. and Fossum, E. R., "Quanta image sensor jot with sub 0.3e- r.m.s. read noise and photon counting capability," IEEE Electron Device Letters, 36(9), 926-928, (Sep. 2015).
[4] Masoodian, S., Rao, A., Ma, J., Odame, K. and Fossum, E. R., "A 2.5pJ/b binary image sensor as a pathfinder for quanta image sensors," IEEE Trans. Electron Devices, 63(1), 100-105, (Jan. 2016).
[5] Chan, S. H., Elgendy, O. A. and Wang, X., "Images from bits: non-iterative image reconstruction for quanta image sensors," MDPI Sensors, 16(11), (2016).

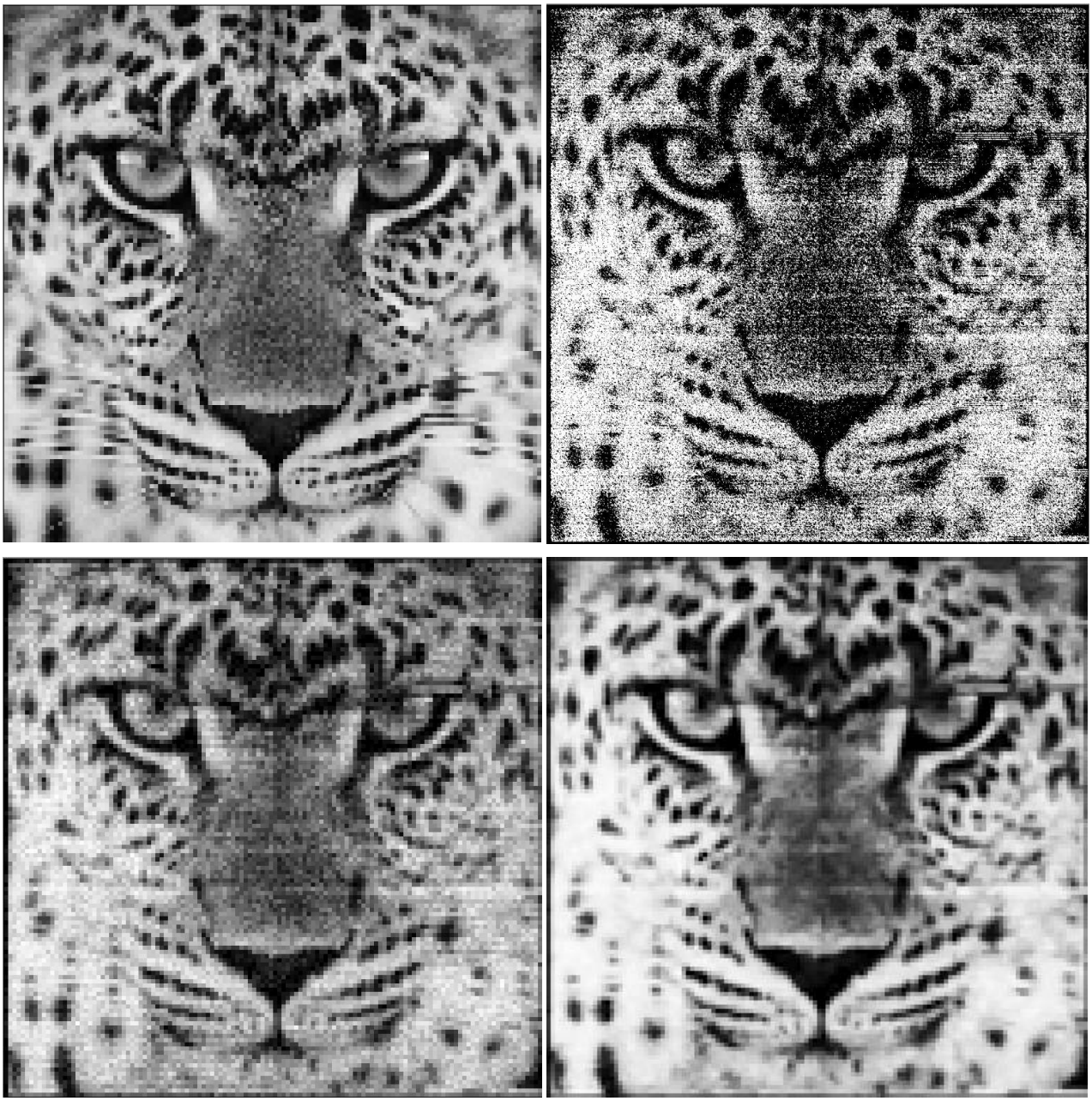

Figure 7. (Upper left) Image of printed scene taken with CMOS image sensor under normal lighting, reduced to 128x128 resolution; (Upper right) One field of binary single-photon data (1024x1024) grabbed from 1Mjot QIS at 1040fps continuous operation from same scene. Some fixed pattern noise (FPN) is observed. (Lower left) Image pixels formed from 8x8x8 cubicle summation from 8 fields of 1Mb data. The resulting image resolution is 128x128. (Lower right) Same QIS data as lower left but processed using Purdue de-noising algorithm [5] for 128x128 resolution.