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A Time-Resolved CMOS Image Sensor with High Conversion-Gain Pixels and Pipelined ADCs

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***Abstract*— This paper presents a CMOS image sensor with high conversion-gain pixels and column-shared pipelined ADCs for Fluorescence-lifetime imaging microscopy (FLIM). Pixel conversion gain of 121 uV/e- is achieved by creating a distal floating diffusion from transfer gate and reset transistor gate without any process modification. 32-channel 10-bit on-chip column-shared pipelined ADCs with sampling rate up to 5MS/s are designed using area-efficient ring amplifiers for the sensor readout. The ring amplifiers are designed based on actively-biased technique which reduces the area further by 40%. This image sensor chip is fabricated in a standard 180nm CMOS image sensor (CIS) process.**

Keywords—CMOS image sensor; fluorescence-lifetime imaging microscopy (FLIM); high conversion gain; pipelined ADC; ring amplifier

I. INTRODUCTION

Fluorescence-lifetime imaging microscopy (FLIM), which visualizes fluorophores based on their intrinsic lifetimes, is a powerful tool in life science research [1]. Image sensors intended for this application are required to have high sensitivity to detect weak fluorescence signals while having accurate time resolution to resolve lifetime on the order of nanoseconds. Single-photon avalanche diode (SPAD) and intensified charge-coupled device (ICCD) are the common sensors of choice, but each has its own limitations. Recent research [2] shows the possibility of designing a CMOS image sensor for this application.

One of the challenges faced by CMOS image sensors in this application is to achieve comparable ultra-low input-referred read noise. This can be solved by increasing pixel conversion gain (CG) to attenuate the read noise from the readout chain including the in-pixel source follower. The benefit of high CG has been demonstrated in [3] with a record low read-noise level of 0.22e- rms in a 65nm process. However, the implementation in [3] requires a customized fabrication process. A new technique to boost pixel CG without process modification is explored in this paper.

Real-time FLIM requires fast image acquisition. Column-parallel ADCs are usually necessary for such high-speed imaging applications. Although single-slope ADCs have a simple circuit configuration [4], their capability in high-speed imaging is limited by the exponential relationship between the number of conversion cycles and the ADC resolution. On the contrary, high-speed ADC architectures, such as successive-approximation ADCs [5], cyclic ADCs [6] and delta-sigma ADCs [7], require much less conversion cycles but consume more area and power. It's nearly impossible to implement a fine layout of such a high-speed ADC in a pitch of one or two columns as pixel size shrinks. To alleviate this problem, column-shared 8-stage pipelined ADCs are used in our design which enables 8 times wider pitch for ADC layout compared to cyclic ADCs at the same data rate. The ring amplifier is chosen for amplification because of its area-efficient design and inherent rail-to-rail output swing. A new actively-biased ring amplifier is introduced to enable further area reduction.

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II. CHIP ARCHITECTURE

The block diagram of the chip architecture is shown in Fig. 1. The image sensor consists of a 256(H)x128(V) pixel array (5um pixel pitch), a clock-tree based global shutter driver, column-parallel programmable gain amplifiers (8x or 16x analog gain), column-parallel S&Hs for correlated double sampling (CDS), a unity gain buffer for analog out, and 32-channel 10-bit pipelined ADCs for digital output.

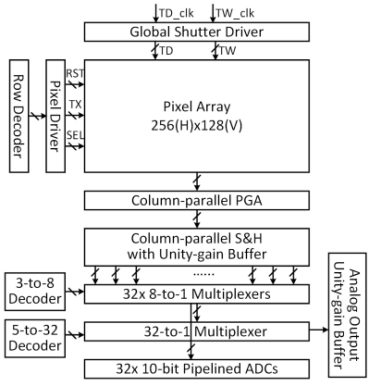

Fig. 1. Chip architecture

III. HIGH CONVESION-GAIN PIXEL DESIGN

In FLIM, thousands of excitation cycles are needed to accumulate enough signals before a readout operation. In order to preserve the photoelectrons collected in previous cycles, it's imperative to have a temporary storage node inside the pixel. In contrast to a traditional 4T pixel, two gates (TD, TW) and an in-pixel pinned storage diode (PSD) are added in our pixel. By controlling TD and TW, the collected photoelectrons in PPD can be modulated to flow in two different directions. When TD

is high and TW is low, the photoelectrons would be drained; when TD is low and TW is high, the photoelectrons would go to PSD. PSD can temporarily store the charges and has a very low dark current generation rate due to its pinned structure. The pixel structure is shown in Fig. 2.

Reducing the parasitic capacitances on the floating diffusion (FD) is critical to increasing pixel CG. In a self-aligned CIS process, overlaps exist between FD and the adjacent gates which are caused by the lateral straggle of the heavy implantation for FD and the lightly-doped drain (LDD) implantation. In deep sub-micron processes, these overlaps add parasitic capacitances to FD which are non-negligible portions of the total capacitance. The parasitic capacitances can be reduced by moving FD away from the adjacent gates. But the heavily-doped P-type PWELL under FD will create big potential barriers in the gaps between FD and the adjacent gates as shown in Fig. 3. To prevent this from happening, a different PWELL (available for buried-channel source follower) is used which has a lightly-doped n- layer on top of the p+ layer. The whole region between TX and RST gates are covered by the buried-channel PWELL. The potential barrier is small when TX or RST is high as shown in Fig. 4. At the same time, the parasitic capacitances are effectively cancelled. Another benefit of this technique is that the FD is still well-shielded by PWELL from the electrons diffused from the substrate. The potential diagrams in Fig. 3. and Fig 4. are obtained by running 2D simulation in TCAD using a real fabrication recipe and the device width (in the direction looking into the cross section) is assumed to be 0.42μm. Although the small barrier will prevent fully charge transfer from PSD to FD when TX is high, the remaining charge would be "pumped" to FD as TX transitions from high to low like the device in [3].

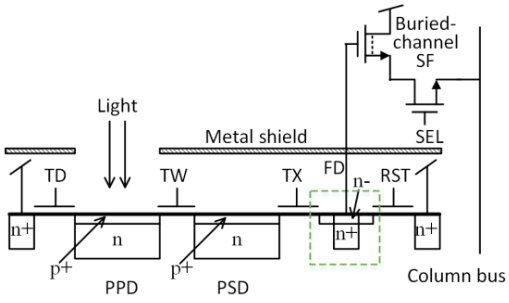

Fig. 2. Pixel architecture

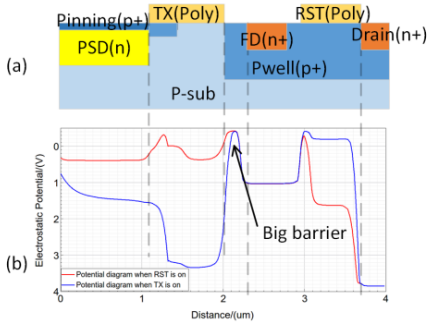

Fig. 3. Distal FD fully-covered by PWELL (a) doping profile, (b) potential diagram when RST is on or TX is on

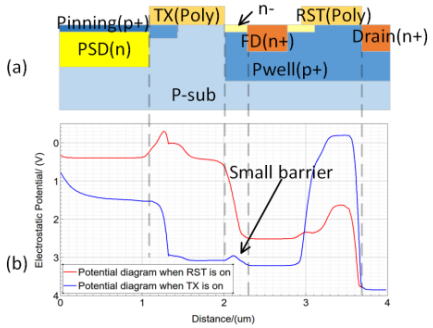

Fig. 4. Distal FD with buried-channel PWELL (a) doping profile, (b) potential diagram when RST is on or TX is on

IV. Pipelined ADC Design

The motivation to choose pipelined ADCs in this design is to achieve a wider ADC layout pitch while maintaining the same frame rate. The operation principle of pipelined ADCs and cyclic ADCs are similar, i.e., amplifying the residual signal with an accurate gain for the next stage or cycle. The difference is that pipelined ADCs trade area for a higher sampling rate. For example, comparing an 8-stage 10-bit pipelined ADC to a single-stage cyclic ADC with the same clock rate, the former has a sampling rate 8 times of the latter but occupies an area around 8 times of the latter. In our design, the pixel pitch is 5um, so the ADC pitch for a pipelined ADC shared by 8 columns is 5x8=40um, which is enough for implementing some layout strategies for better transistor or capacitor matching. Further area saving is possible as the latter stages in a pipelined ADC requires less accuracy. The structure of the designed pipelined ADC is shown in Fig. 5, the input sampling capacitors are reduced gradually for each stage.

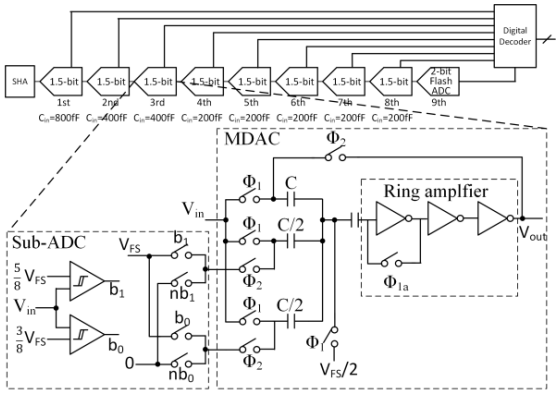

Fig. 5. Pipelined ADC structure

Ring amplifier based MDAC has been proposed in [8] for pipelined ADCs. The appealing features of a ring amplifier includes high-speed slew-based settling, rail-to-rail output swing, and scalability for process scaling. Derived from the same concept, a self-biased ring amplifier is proposed in [9] by generating offset with a large resistor in the 2nd stage. To create a more area-efficient solution which is critical to CMOS image sensor design, we introduce the actively-biased ring amplifier with a new technique to generate the offset.

Fig. 6 shows the self-biased ring amplifier from [9] and the actively-biased ring amplifier side by side. In the self-biased ring amplifier, as current goes through R_{BIAS}, a voltage drop is created from V_{CP} to V_{CN}. At steady state, V_{CP} should be high enough to turn off M_{3P} and V_{CN} should be low enough to turn off M_{3N}. The large resistor is replaced by a pair of PMOS and NMOS in the actively-biased ring amplifier. The gates of PMOS and NMOS are tied to reference voltages which are tunable. In the actual design, V_{BP} is set to ground and V_{BN} is set to positive supply.

Fig. 7 shows the conception of this new structure step by step. The gist of generating the offset in the 2nd stage is to generate a high voltage V_{CP} at the drain of M_{2P} and a low voltage V_{CN} at the drain of M_{2N}. If we think of M_{2P} as a current source at steady state, V_{CP} can be set by using a cascode transistor M_{BP}. The sizing of M_{BP} is determined by bias current and desired voltage. Similar steps can be followed to add M_{BN} on top of the bottom transistor M_{2N}. If we stack the two parts in Fig. 7(a) together, we'll get a structure shown in Fig. 7(b) which is essentially a high gain inverter-based amplifier. The voltage headroom is limited and the voltage at the drains of M_{BP} and M_{BN} is not well-defined unless it's put in a negative feedback loop. The solution presented here is connecting M_{BP} and M_{BN} back to back as shown in Fig. 7(c). By doing so, V_{CP} and V_{CN} are defined by M_{BP} and M_{BN} respectively. Proper sizing of M_{BP} and M_{BN} is needed to ensure that the static currents flowing through them are balanced.

The resolution of a ring amplifier is determined by its dead zone which is defined as the input voltage range to turn off both transistors in 3rd stage. Fig. 8 shows the results of running DC sweeps of V_{in} vs. I_{out} for a self-biased ring amplifier and an actively-biased ring amplifier. Both amplifiers have the same size of dead zone around 600uV. The self-biased ring amplifier requires a 30k ohms resistor to generate the offset. With a sheet resistance of several hundreds of ohms, a 30k poly resistor would have an area of about several hundreds of um^2. In contract, the MOSFET pair in our design only takes up about 25 um^2 area which is only 1/10 of resistor. The total reduction of area for ring amplifier is about 40%.

Another difference revealed in Fig. 8 is that the actively-biased ring amplifier has a sharper transition at the both edge of dead-zone which affects its settling behavior in stabilization process. Fig. 9(a) shows the amplification phase of a transient simulation. Both types of ring amplifiers have about the same initial slewing speed. Fig. 9(b) gives a zoom-in view in the stabilization process. A higher first overshoot and a shorter final settling time are observed for actively-biased ring amplifier. This is because it has a higher output current in the "weak" dead-zone for the same overshoot voltage.

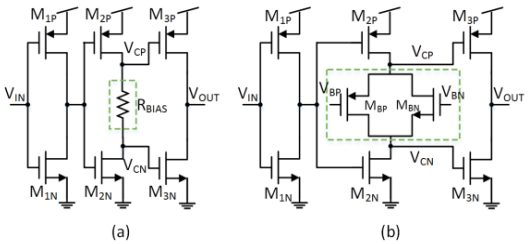

Fig. 6. (a) Self-biased ring amplifier, (b) actively-biased ring amplifier

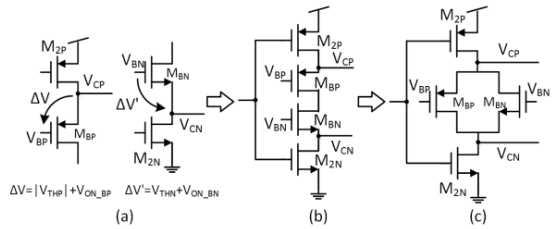

Fig. 7. Illustration of the conception of actively-biased ring amplifier (a) adding cascode transistors, (b) a cascode inverter-based amplifier, (c) 2nd stage of actively-biased ring amplifier

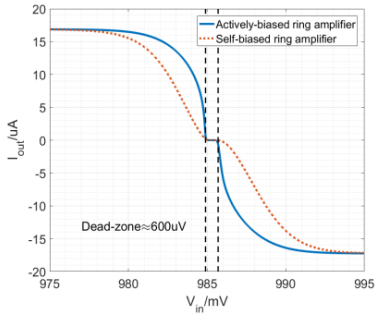

Fig. 8. DC sweep results of V_{in} vs. I_{out} for ring amplifiers

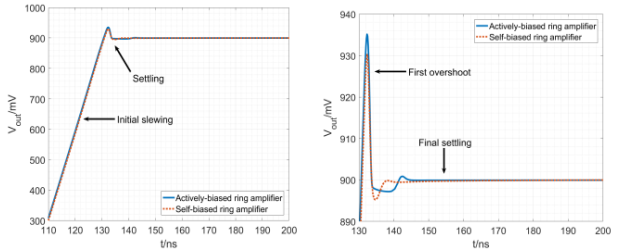

Fig. 9. (a) Ring amplifiers' output voltage in amplification phase, (b) zoom-in view of stabilization process

V. Measurement Results

The CG of the designed pixels is measured at 121uV/e- using the photon transfer curve method as shown in Fig. 10. It's about 73% higher than a baseline pixel with a typical value of 70uV/e-.

The pixel's charge modulation operation is tested with a pulsed light source. TW and TD are set to the same pulse width of 500ns. The light pulse is delayed with a step of 10ns. The acquired signals are shown in Fig. 11. The nonlinear portion is caused by the different propagation delays of the light source driving signal and TW, TD. It's expected to be avoided with a finer adjustment of the delays.

The measured DNL/INL vs. output code for the pipelined ADC is plotted in Fig. 12. The power consumption breakdown for one pipelined ADC is shown in Fig. 13.

VI. Conclusion

A time-resolved CMOS image sensor designed for FLIM application is presented. A new technique to increase CG by using buried-channel PWELL is discussed. This technique has

the advantage of requiring no process modification. A new tunable actively-biased ring amplifier with 40% area reduction is introduced and implemented in the column-shared pipelined ADCs. A sample image taken with the image sensor under low-light condition is shown in Fig. 14. A picture of the fabricated image sensor chip die is shown in Fig. 15.

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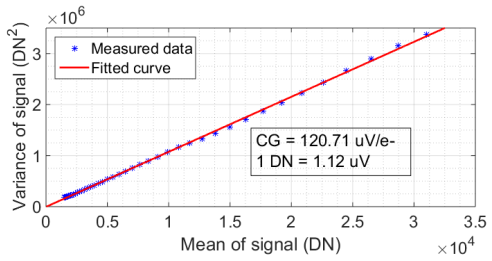

Fig. 10. Measured photon transfer curve

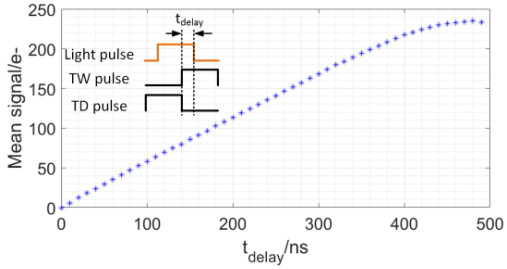

Fig. 11. Acquired signal with pulsed light source for different time delays

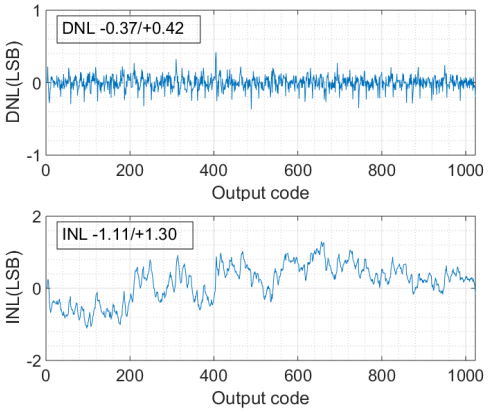

Fig. 12. Measured ADC DNL/INL

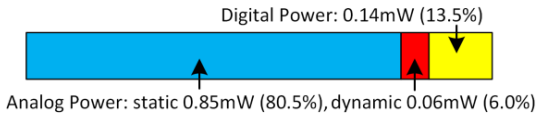

Fig. 13. Power consumption breakdown for one pipelined ADC

Fig. 14. Image taken with designed sensor in low-light condition (~200e-)

Fig. 15. Photo of the fabricated image sensor chip die

Table 1. Chip summary

Pixel Array	256(H)x128(V)
Pixel Pitch	5um
Pixel Conversion Gain	121 uV/e-
Read Noise	2.52 e- rms (median)
ADC Resolution	10bit
ADC Supply	1.8V
# of ADC Channels	32
ADC Sampling Rate	5MS/s
Input Range	0.1V-1.7V
DNL	-0.37/+0.42
INL	-1.11/+1.30
ADC Power	1.05 mW/channel
Chip Total Power	228 mW

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