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Experimental Comparison of MOSFET and JFET 1.1μm Pitch Jots in 1Mjot Stacked BSI Quanta Image Sensors

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***Abstract*— This paper reports on the design, characterization and comparison of MOSFET and (for the first time) JFET-based QIS readout. Each type of specialized pixel (or "jot") was realized in a 1Mjot array, and 20 different 1Mjot arrays were fabricated together on one stacked BSI chip (20Mjot total).**

I. Introduction

The quanta image sensor (QIS) was proposed in 2005 [1, 2]. A QIS may contain hundreds of millions to billions of specialized pixels, called "jot". The jots detect the number of incident photons and output single-bit or multi-bit counting signal. The QIS image can then be created from jot data by image processing.

The read noise of an image sensor determines its capability of photoelectron counting. Deep sub-electron read noise (DSERN) is required for photoelectron counting [3], corresponding to input-referred read noise of 0.5e- r.m.s. or lower. To realize accurate photoelectron counting with an ideal counting error rate, the read noise of 0.15e- r.m.s. is ultimately desired for QIS applications. In a QIS-type readout circuitry, the in-jot source follower (SF) is the major contributor of read noise. Approaches of eliminating QIS read noise include enhancing the conversion gain (CG) on the floating diffusion (FD) node and reducing the voltage noise from the SF.

The pump-gate jot with tapered reset (TPG) was proposed by our group to enhance the CG of jots to the range of 400μV/e-. In 2015, the read noise of 0.22e- r.m.s. was demonstrated with this technique in a small 32x32 test array, and it was for the first time the photoelectron counting capability was demonstrated without using avalanche gain at room temperature [4, 5]. The previous results motivated us to merge the PG jot with the QIS-type readout in a more sophisticated sensor system. To achieve this goal, a prototype chip which contains 20 different 1Mjot arrays was designed and fabricated in TSMC 45nm stacked BSI process. Among the 20 arrays on this chip, different jot designs and readout architectures are tested. For the further reduction of the read noise towards 0.15e- r.m.s., several new jot concepts are implemented based on the previous PG jot design, including a JFET-based in-jot SF and a punch-through reset (PTR) diode. Thus, a best-case read noise of 0.17e- r.m.s. was demonstrated. In this paper, the characterization results of MOSFET and JFET jots with and without PTR will be discussed and compared.

II. Jot Design and Concept

As mentioned, the QIS read noise can be reduced by improving the CG of the FD and reducing the SF voltage noise. Following the two paths, the following topics are investigated with the prototype chip.

- The comparison of the voltage noise of buried-channel (BC) MOSFET SF and surface-channel (SC) MOSFET SF.
- The improvement of CG by PTR.
- The comparison of the voltage noise of JFET-based SF and MOSFET SF.
- The improvement of CG by JFET SF.

To address these topics, 8 major types of jots are implemented: (1) TPG jot with SC MOSFET SF; (2) TPG jot with BC MOSFET SF; (3) PTR jot with SC MOSFET SF; (4) PTR jot with BC MOSFET SF; (5) TPG jot with SC JFET SF; (6) TPG jot with BC JFET SF; (7) PTR jot with SC JFET SF; and (8) PTR jot with BC JFET SF. Each type of jot also contains several small variations both in the layouts and the implantations. The simplified layouts of the jots are depicted in Fig. 1. Note that all the jots use a 2-way shared readout architecture and have a pitch size of 1.1μm. They also share the same design in the portion of the pump-gate photodiode. As shown in Fig. 1, the pump-gate photodiode doping profile is adopted from the previous demonstrated design and optimized for an improved effective fill-factor and better response in the shorter wavelength regime. The doping profiles of the JFET SF are shown in Fig. 2. The design details of this device can be found in [6]. This device has a p-type channel, and the potential of the gate, or the FD, modulates the channel cross-section depletion area and thus controls the voltage on the source terminal. When the source is biased by a constant current source, the device works as a source follower. The JFET SF can effectively reduce the parasitic FD capacitance from the SF gate, hence leads to an improved CG. On the other hand, it can reduce the interaction between the channel carriers and the surface interface traps, which is widely believed to be the major source of the SF 1/f noise and RTS noise [7, 8]. From these two aspects, the read noise is expected to be further reduced. In Fig 2(d), the doping profile of a PTR diode is presented. It is used to eliminate the overlap capacitance between the FD and the reset gate (RG), thus further improving CG. In this device, the FD is reset by applying a relatively high voltage on the reset drain (RD) node. As the depletion region

of the RD extended with higher bias, the "punch-through" occurs when the p-type region between the FD and the RD is fully depleted. A current path is created under this condition and the FD is discharged. Except for the reset phase, the RD is biased by a relatively low voltage to maintain a potential barrier between the FD and the RD to shut down the current path. The design details and simulation results can also be found in [6]. The initial PTR technique was developed at Kodak in 1996 to eliminate the reset noise in CMOS image sensors (CIS) and to achieve a faster global reset over the entire array of pixels [9]. Recently, it was also applied to CIS for the improvement of CG. Note that limited by the high full-well capacity (FWC) required by CIS, a bias voltage as high as 25V is needed for the PTR process, as suggested in [10]. Since the high voltage is not compatible with regular CMOS process, the application is constrained, so the bootstrapping technique was applied to reduce the voltage needed for the gateless reset, and a CG of 172μV/e-was achieved [11]. PTR is a perfect fit for QIS applications due to the small FWC needed by jots. The implementation of PTR technique in QIS started in 2015 at Dartmouth [12], and the PTR diode for QIS can accomplish the reset process with a much lower voltage (e.g. 2.5V).

III. Characterization Results

The simplified schematic of the analog readout chain is shown in Fig. 4. Each column output line is connected to a correlated double sampling (CDS) circuitry. The output of every 4 CDS units are selected by a multiplexer and sent to a unity-gain buffer. The buffered signal is then amplified by a switch capacitor programmable gain amplifier (PGA). Another unity-gain amplifier is used to drive the output pad after the PGA. For the best noise performance, correlated multiple sampling (CMS) was used to suppress the noise in the readout chain, where 20 CMS cycles of signal were collected in series. It was found that further increased cycles could not reduce the read noise, probably because of the addition of low-frequency noise due to the extended readout process.

The CG and read noise were characterized with photon counting histogram (PCH) method [13]. In this measurement, the PCH of each jot was created from 20k continuous reads. The read noise was extracted from the valley-peak-modulation (VPM), and the CG was extracted from the peak-to-peak distance. The inevitable variability in the fabrication process always leads to the performance variation of each jot. For example, small misalignments of masks may lead to the variation of CG, and the randomness in the number of defects in each jot may lead to different voltage noise magnitude. Since the analog readout speed is currently limited on the testing board, about 7k jots of each type were tested. The histograms of the output-referred CG (after in-jot SF) are shown in Fig. 5. A 2-3% variation of CG is observed in the jots with MOSFET SF. Among the 4 types of jots, because of the elimination of the RG overlap capacitance on the FD, the CG of PTR jots is about 10% higher than the TPG jots (~370μV/e- over ~340 μV/e- in average). Note that the BC or SC SF has negligible impact on the CG, which suggests that the two types of SF have similar gain.

The histograms of read noise are exhibited in Fig. 6. Thanks to the higher CG, the PTR jots also demonstrated lower read noise compared to the TPG jots (0.21e- r.m.s. over 0.23e- r.m.s. in average). Among the 14k tested PTR jots (BC and SC), several best performed jots were found to have a record-low read noise of 0.17e- r.m.s., and the PCH of one "golden" jot is shown in Fig. 8. Note that a relatively long tail was observed in the read noise distribution, and the jots with high noise were found to have stronger high-frequency noise. Further investigation is needed to discover the source of noise, but the suspicion is RTS noise. BC SF exhibited minimal advantage over SC SF in terms of a slightly shorter tail in the read noise distribution and a smaller read noise variation (15% over 16%). However, the effectiveness of noise reduction from BC MOSFET SF is lower than expected. The scatter plots of CG versus read noise in voltage are shown in Fig. 7. The plots suggest minimal correlation between CG and read noise, and show the random variation between devices.

The SC JFET has been observed to have relatively low SF gain due to weak pinch-off effect. It has been believed to be caused by some current leakage path through the bulk of silicon. The BC JFET has higher SF gain, but the gain was found to have a larger variation compared to MOSFET. Some best performed JFET jots showed significantly high CG (500-600μV/e-), and photon counting histograms were demonstrated from those jots, as shown in Fig. 9. However, the voltage noise from the SF is also higher than MOSFET, which compensates the reduction of read noise from higher CG. The strong noise is believed to be related to the bias condition of the JFET, and the noise sources are under investigation.

IV. Summary

In this paper, several new jot concepts and device design are introduced, including a JFET-based in-jot SF and a punch-through reset (PTR) diode. The characterization results of those devices are discussed and compared.

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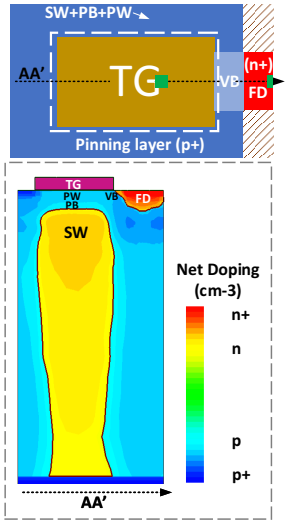

Figure 1: Simplified layout of and simulated doping profile of the pump-gate photodiode.

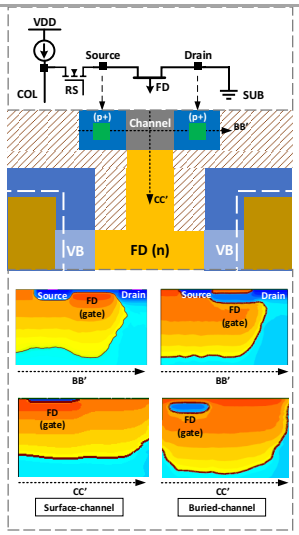

Figure 2: Simplified layout of and simulated doping profile of the JFET SF.

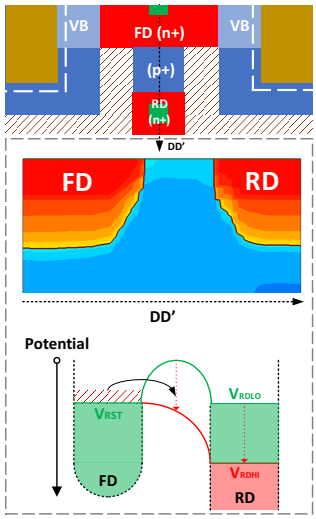

Figure 3: Simplified layout of and simulated doping profile of the punch-through reset diode.

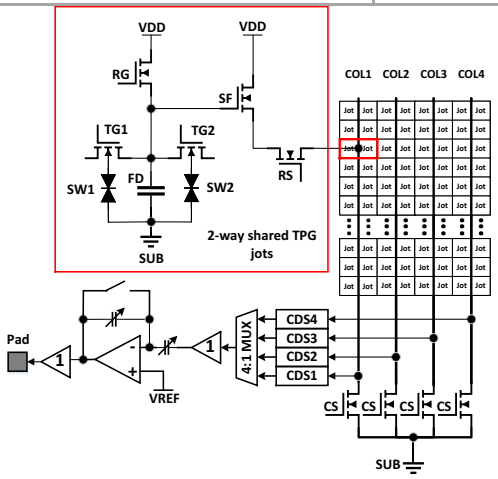

Figure 4: Simplified schematic of one on-chip readout unit.

Table 1: Characterization Results

	TPG SC	TPG BC	PTR SC	PTR BC	JFET
CG Mean (μV/e-)	347.2	345.1	362.5	367.8	
CG Var.[1]	2.91%	2.56%	2.23%	2.59%	
RN Mean @RT (e- r.m.s.)	0.235	0.236	0.219	0.216	
RN Var.[1]@RT	16.3%	15.7%	16.3%	15.3%	
Dark Current @RT					
Process	TSMC 45nm/65nm stacked BSI				
Pixel Pitch	1.1μm				
Readout	2-way shared readout				

[1] variation stands for the ratio of standard deviation over mean

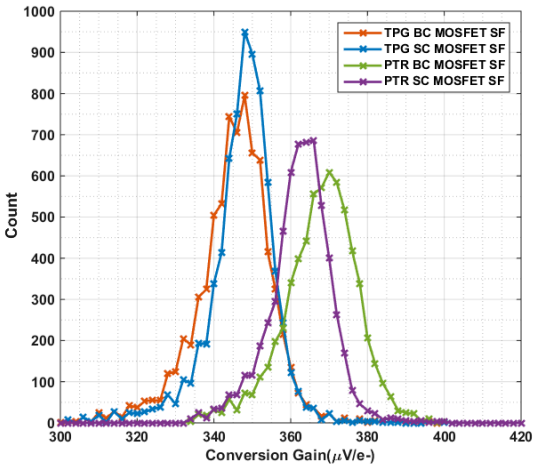

Figure 5: Histograms of CG from TPG and PTR jots.

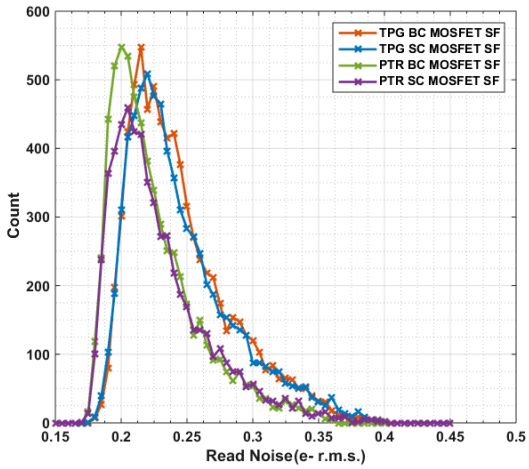

Figure 6: Histograms of read noise from TPG and PTR jots.

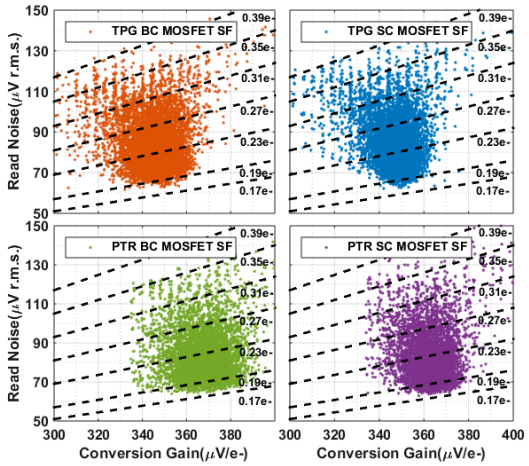

Figure 7: Scatter plot read noise vs. CG from TPG and PTR jots.

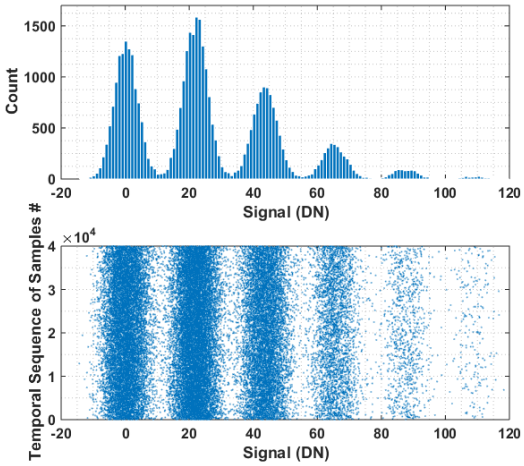

Figure 8: (top) PCH from the golden PTR jot. The read noise is 0.170e- r.m.s. and the quanta exposure H equals to 1.14. (bottom) The scatter plot of the 40k PCH samples versus their temporal sequence.

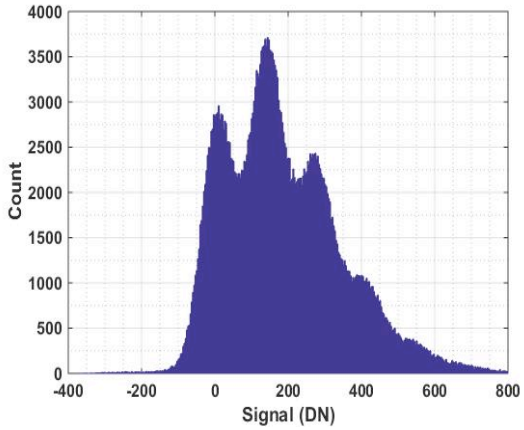

Figure 9:PCH from a JFET jot.

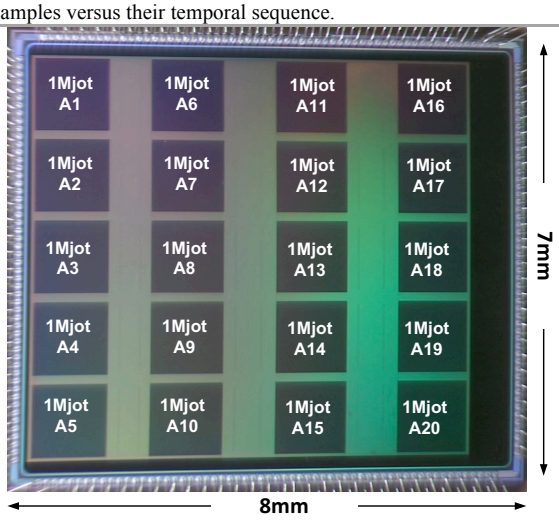

Figure 10: Photo of the prototype chip.