Accepted for publication, IEEE Trans. Electron Devices Special Issue on Solid-State Image Sensors. Expected print publication Feb. 2016.

A 2.5pJ/b Binary Image Sensor as a Pathfinder for Quanta Image Sensors

Saleh Masoodian, *Student Member, IEEE*, Arun Rao, *Student Member, IEEE*, Jiaju Ma, *Student Member, IEEE*, Kofi Odame, *Member, IEEE*, and Eric R. Fossum, *Fellow, IEEE*

***Abstract*— This paper presents a pathfinder binary image sensor for exploring low-power dissipation needed for future implementation of gigajot single-bit QIS devices. Using a charge-transfer amplifier (CTA) design in the readout signal chain, and pseudo-static clock gating units for row and column addressing, the 1Mpixel binary image sensor operating at 1000fps dissipates only 20mW total power consumption, including I/O pads. The gain and ADC stages together dissipate 2.5pJ/b, successfully paving the way for future gigajot QIS sensor designs.**

***Index Terms*—analog to digital converter (ADC), charge transfer amplifier (CTA), comparator, quanta image sensor (QIS), readout circuit.**

I. Introduction

QUANTA image sensors (QIS) are proposed as a paradigm shift in image capture to take advantage of shrinking pixel sizes [1]. Fig. 1 shows the concept of QIS. The key aspects of the single-bit QIS involve counting individual photoelectrons using sub-diffraction-limit-sized, spatially-oversampled binary photodetectors, called jots, at high readout rates, representing this binary output as a bit cube (x,y,t) and finally processing the bit cubes to form high dynamic range images.

The challenges to realize the QIS have been addressed in [2] and imaging performance analyzed in [3]. The binary photodetector, 'jot', requires a sub-micron pitch for a gigajot implementation. In addition, the jot needs to demonstrate high conversion gain and quantum efficiency (QE). The collected photoelectrons should produce at least a 1mV/e- signal on the column bus for reliable detection by the readout circuits. The single-photon avalanche diode (SPAD) was introduced as a possible jot candidate in [4] [5] [6]. A large pitch (>5µm) due to intrapixel circuits, and large dark current are the main drawbacks today of a SPAD-based jot. Other jot candidates have been explored, such as a BJT-type jot [7], single-electron field-effect transistor (SEFET) [8], and the pump-gate jot device which looks very promising [9] [10]. The sub-diffraction-limit pitch of the jot device will make it more susceptible to crosstalk and this effect will be more pronounced with color filters included. A few studies to address the color issues related to QIS are mentioned in [11] [12] [13].

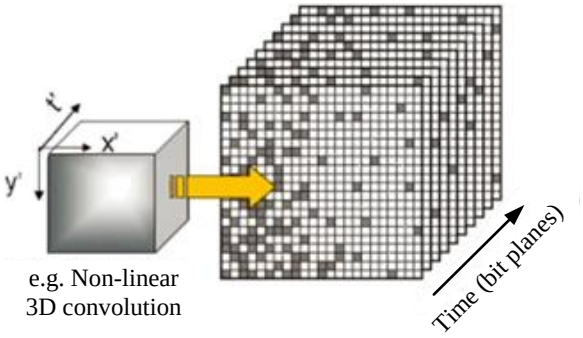

Fig. 1. QIS concept.

The principal challenge addressed in this paper is the design of internal high-speed and low-power addressing and readout circuitry. A QIS may contain over a billion jots, each producing just 1mV/e- of signal, with a field readout rate 10-100 times faster than conventional CMOS image sensors.

For example, in a 1000 fps gigajot QIS with 16:9 aspect ratio, there would be 42,000 columns, with 24,000 jots in each column. Use of conventional CMOS imager readout circuits would result in high power dissipation and impact sensor performance.

To implement the single-bit QIS ADC, the inherent random offset in a comparator and latch circuit must be overcome. This traditionally requires additional gain and concomitant power dissipation. Minimizing the power dissipation in the readout was one of the goals of this work and was achieved using a 4-stage charge-transfer amplifier (CTA). Additional power savings comes from the exploration of pseudo-static circuits with clock gating units in the digital row addressing and column circuits. Use of a partially-pinned photodiode with modified implants to increase conversion gain was also explored.

Use of these techniques implemented in a pathfinder test chip has resulted in a significant improvement in an energy-per-bit figure of merit compared to previous work. The techniques developed may have application to conventional CMOS image sensors that require minimal power dissipation.

II. Sensor Architecture

The 1376(H)x768(V) pixel image sensor uses a partially-

Manuscript submitted on 18th April 2015. This research was sponsored by Rambus Inc. A portion of this work was presented at IISW 2015.

All the authors are with the Thayer School of Engineering at Dartmouth College, Hanover, NH 03755 USA (e-mail: saleh.masoodian.th@dartmouth.edu).

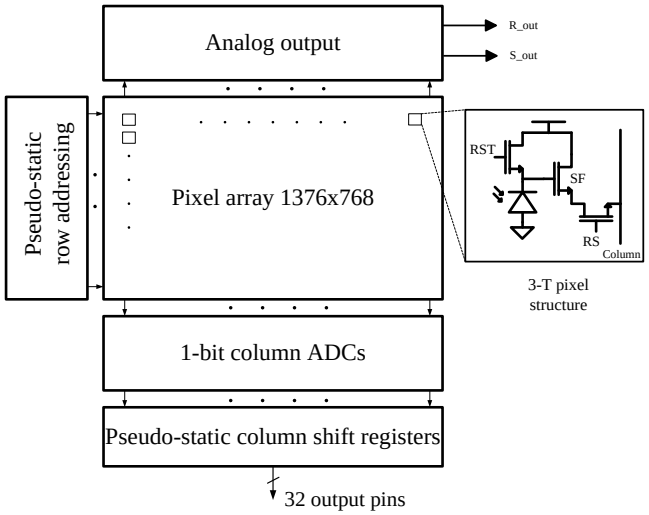

Fig. 2. Architecture of the 1MP pathfinder image sensor.

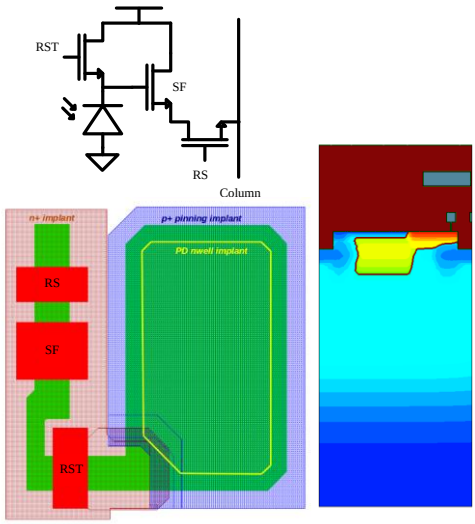

Fig. 3. Schematic, layout and simulated doping profile of the pixel.

pinned photodiode, 3.6µm 3T pixel, and readout architecture implemented in the X-FAB 0.18µm process, as shown in Fig. 2. The sensor is operated in a single-row rolling-shutter mode so true correlated double sampling (CDS) can be utilized. This means that when a particular row is accessed, it is first reset, allowed to briefly integrate a signal, and then read out before moving to the next row. However, to achieve 1000fps, this leads to extremely short integration times (i.e. <1 µs), useful only in the lab. To characterize the pixels, lower frame rates were used as explained in Section VI.

A column-parallel single-bit ADC using a CTA-based design detects a minimum 0.5mV output swing from the pixel. The ADC is capable of sampling at speeds of 768kSa/s. The sensor operates at 1000fps, which corresponds to a row time of 1.3µs, a signal integration time, T_{int}, of 0.9µs, and an output data rate of 1Gb/s.

Shift-register-based row and column-addressing circuits are designed with pseudo-static flip-flops and clock gating units. Additionally, an analog output port was included on top of the pixel array so that the pixels could be directly accessed and characterized.

III. Pixels

A 3T pixel with partially-pinned photodiode [14] was utilized. Actual jot implementation requires a smaller technology node and that work is underway separately. 4T pinned-photodiode pixels were not yet available in this process at the time of tapeout. With a 3T pixel, use of CDS for low read noise requires single-row integration times. A 4T pixel, if available, would have allowed CDS with longer integration times.

The schematic and the layout of the pixel are shown in Fig. 3. The 3T pixel is front-side illuminated, with a pitch of 3.6µm, and design fill-factor of approximately 45%. The nominal conversion gain of the fab-provided pixel was 57µV/e-.

To increase the conversion gain and reduce read noise (in electrons), the pixel was slightly modified. The pixel was designed and simulated using Synopsys TCAD tools. As shown in Fig. 3, the partially-pinned photodiode contains two parts. One part is the lightly doped n-well underneath the p+ pinning layer, and another is the n+ output node. The lightly-doped n-well is made deeper than the n+ node to have a higher sensitivity in longer wavelength photons and helps collect photoelectrons and channel them to the n+ node. The dose of the p+ pinning layer was also modified accordingly. It ensures that the n-well underneath has a very low V_{pin}, and can be completely depleted. It also helps shield the Si-SiO_2 interface traps, which reduces the dark current and improves blue light sensitivity. The lightly-doped n-well has a small junction capacitance per μm^2 but a bigger area size, and the n+ output node has a high junction capacitance per μm^2 but a smaller area size. Relatively, the n+ node contributes most of the total capacitance. The doping of the n+ output node has to be high enough to make an ohmic contact, so only the doping of the lightly-doped n-well was reduced. However, it still helps reduce the total output capacitance and achieve a higher conversion gain. The TCAD simulation yields 119µV/e- conversion gain and 9,500e- FWC, which matches subsequent measurement results.

IV. Column ADC

The 1376 columns in the imager array are biased using a current source at the bottom of each column. The 768 pixels on each column present significant capacitance on the column bus and the value of current chosen determines the settling time on each column. Fig. 4 shows the simplified schematic of a single column. The analog output block in the top section consists of a simple correlated double sampling (CDS) circuit and source-follower buffers.

A column-parallel 1-bit ADC detects a 500µV change (corresponding to ~5.8 e-) on the column bus. As Fig. 5 shows, the 1-bit ADC circuit comprises a cascade of 4 fully-differential CTA sense amplifiers, followed by a D-Latch comparator (A single-ended CTA was first introduced in [15].). Transistor mismatch in the comparator produces offset

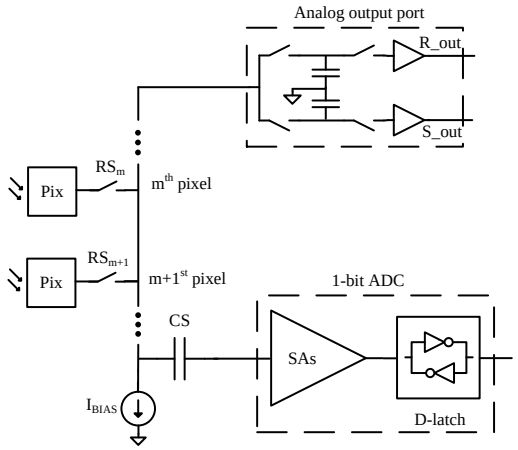

Fig. 4. Simplified readout circuit schematic for a single column of pixels in a single-bit QIS.

in the circuit, but the CTAs provide a total gain of 400V/V, which reduces the input-referred offset to less than 500μV, or half a V_{LSB}. Any offset due to the CTAs themselves is minimized by resetting and precharging them during each sample, without the need for explicit auto zeroing. A detailed description of the differential-CTA operation can be found in [16] [17].

Compared to [17], in which a single-ended CTA was used, use of a differential CTA and column-parallel ADC layout in this image sensor requires more power dissipation. The gain of the CTA is approximately the ratio of C_t to C_o, where C_t is a drawn capacitor (see Fig. 5) and C_o is the CTA's load capacitance. To fit within the narrow pitch of the pixel, a large value of C_t is possible only if it is drawn with a very high aspect ratio. This would in turn require long metal routing lines, which unfortunately produce parasitic capacitances that increase C_o. Thus, the C_t/C_o ratio would be reduced, effectively diminishing the advantage of having drawn a large C_t in the first place. The constraints of the narrow pixel pitch mean that the gain in a single CTA stage is limited to approximately 4.5 V/V; a cascade of 4 CTA stages is needed to achieve a total gain of 400 V/V.

Sensor readout is essentially rolling shutter with single-row integration time to allow CDS with 3T-pixels. Following row selection, the pixels are reset while the CTAs in the ADCs are reset then precharged, and the D-latch comparator enters the latch and then reset phase. After pixel resetting, the integration period is started. During the integration period, the D-latch comparator is in the transfer phase, while the CTAs are in the amplify phase, tracking and amplifying any voltage changes on the column. A DC-blocking capacitor is used between the column and ADC, in order to set the ADC input to V_{pre} and shield it from differences in common mode due to threshold voltage mismatch in the pixels' source-followers. Due to the structure of the CTA, no sample and hold circuits are needed to store the reset and signal levels. The output of the photodiode is sampled (integrated) onto the CTAs' capacitors, simultaneously. As mentioned above, the current source at the bottom of each column is used to bias the large parasitic column capacitance that comes from the row-select switches on the column, and to provide the required settling

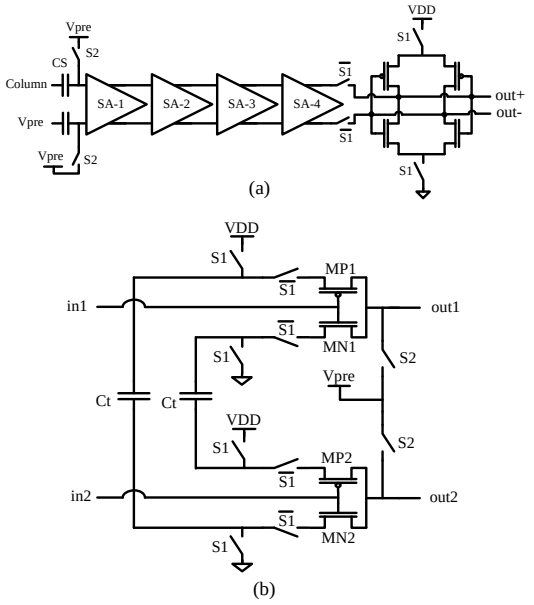

Fig. 5. (a) 1-bit ADC (shown in Fig. 4) based on a cascade of sense amplifiers and a single D-latch comparator. (b) Schematic of each sense amplifier that is implemented as a differential charge transfer amplifier.

time. At the end of the integration period (or amplify phase of the CTA), the D-latch comparator is in the latch phase, and it will flip state depending on whether or not the column voltage has changed by more than 500μV. The final state of the comparator is saved in a dynamic flip-flop to be sent off-chip by column shift registers and multiplexers. The timing and signal waveforms of the functioning of one column and ADC are shown in Fig. 6. Note that for 4T-type pixels, the same general timing would be used, with the integration period replaced with the signal transfer from the PPD to the FD phase. For a gigajot QIS, where more advanced processes such as 45nm might be used so that the pitch of the jot would be sub-micron, the proposed structure can be used by putting ADCs on both top and bottom sides of the jot array, and/or multiplexing a group of columns to one ADC.

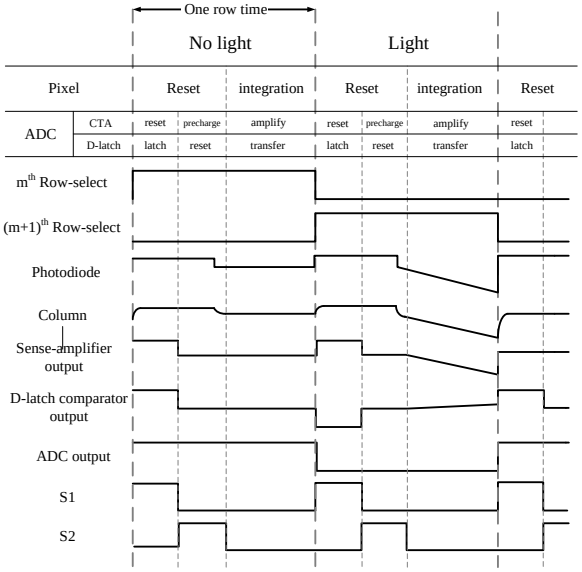

Fig. 6. Timing diagram and various phases of operation for each column and ADC.

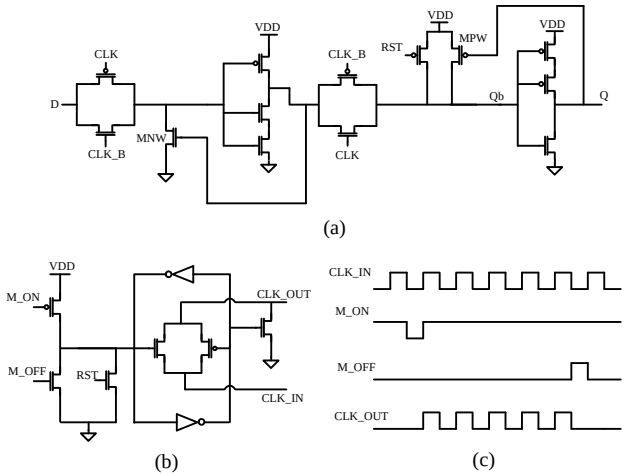

Fig 7. (a) Pseudo static flip flops and (b) clock gating units used in the row addressing and column shift register circuits, with (c) timing diagram.

V. Row and Column Addressing Circuits

Besides the readout signal chain and ADC, a second concern in a gigajot QIS is clock distribution power in the row selection circuits. To address this concern, a tree structure of clock gating units is used, whereby power is conserved by distributing the clock to only the active sections of the shift registers [18]. As shown in the schematic of Fig. 7, the M_ON and M_OFF transistors of the clock gating units are controlled by the outputs of the flip-flops in the shift registers. These flip-flops are implemented as pseudo-static circuits, which combine the low power consumption of a dynamic circuit with the robustness of a static one. The pseudo-static flip-flop is based on a dynamic flip-flop that has been modified with weak feedback transistors, MPW and MNW, to prevent destructive charge leakage. Fig. 7 also shows the clock gating unit, along with a timing diagram. The column shift registers are based on pseudo-static flip-flops too, and they serially transfer the ADC outputs off chip, at a rate of 33 Mbps. To conserve pin count, 43 columns are multiplexed onto each output pin.

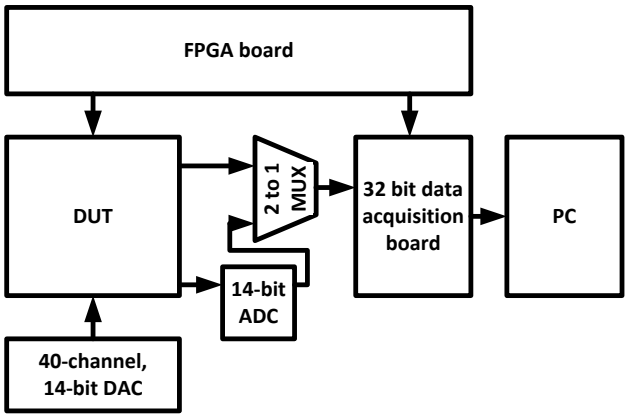

Fig. 8. Test setup block diagram.

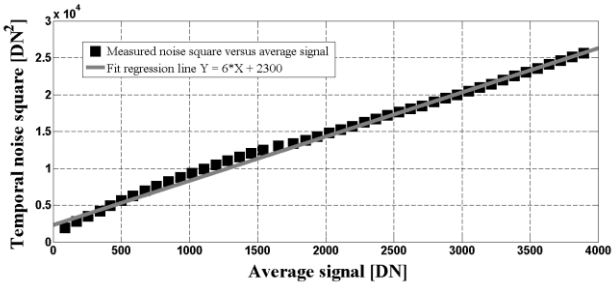

Fig 9. Measured temporal noise squared versus average signal.

VI. Implementation and Experimental Results

A PCB was designed to completely characterize the image sensor and designed readout circuits. The image sensor is mounted on the PCB using a 256 pin PGA package. Peripheral components such as DAC, ADC, and connectors to FPGA and data acquisition boards were soldered onto the PCB. Fig. 8 shows the block diagram of the test setup. Additionally a light source with uniform intensity to illuminate the pixels was used.

As described in Section II, the imager has one analog output port and 32 digital pins with an output data rate of 33Mb/s on each pin. A 600MB/s, 32 channel data acquisition board [19] was used to grab the digital data from the imager and send the data to a PC for further processing.

To produce accurate DC voltage levels for the imager circuits, a high precision 14-bit, 40-channel DAC was used. Outputs of the channels of the DAC are buffered by unity gain amplifiers to provide sufficient current. An Atlys FPGA development board [20] generates synchronized control signals for the imager, data acquisition board and peripheral components. LVDS signaling protocols were utilized for high-speed digital signals.

To characterize the pixels, a 14-bit ADC quantized the amplified output of the analog port of the image sensor. The imager was uniformly exposed to the light source. The pixels' data was captured for 45 different exposure times, ranging from 1µs to 100µs by changing frame rate, with 1500 samples for each exposure time. Variance was plotted as a function of signal (in DN) and a straight line relationship was obtained, as expected for photon shot noise (Fig. 9). From the slope, the output-referred conversion gain is obtained as 6.0 DN/e-. From calibration of off-chip circuits, their gain is 8.63µV/DN.

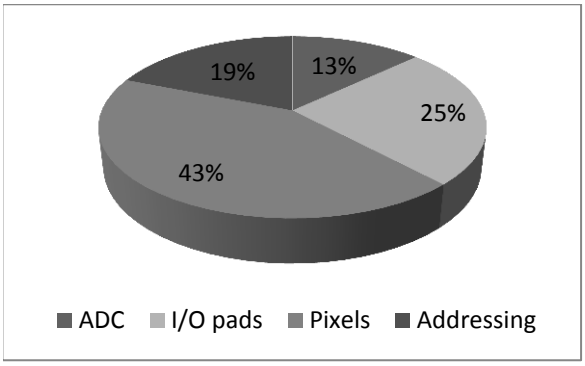

Fig. 10. Power breakdown of the imager chip.

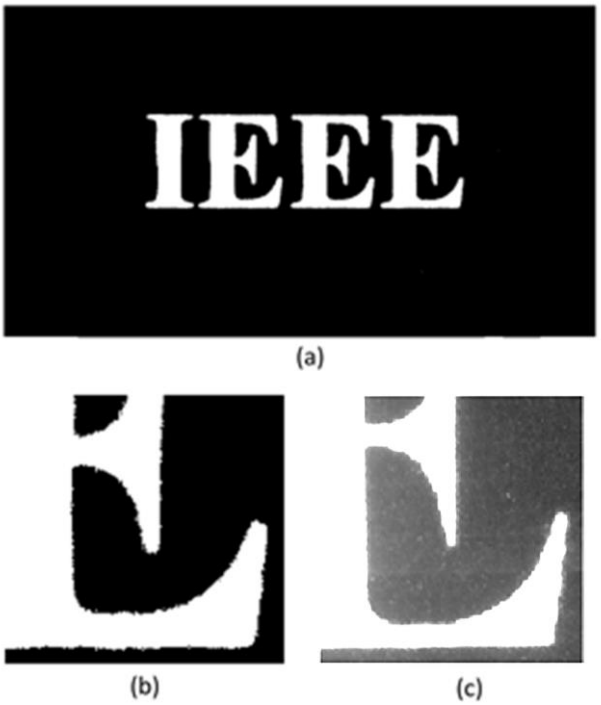

Fig. 11. (a) Single captured binary frame, (b) Blowup of binary frame to show more details as described in text, (c) Image of the object taken by a digital camera under microscope.

Using simulated circuit values for the gain of the pixel source-follower (0.721 V/V) and the pad driver SF (0.605 V/V), the input-referred conversion gain of the pixel was determined to be 119μV/e-. Measurement results show the noise on the column under dark conditions is 240μV r.m.s. or 2e- r.m.s.

The row addressing shift register was implemented with dynamic flip-flops that were modified with weak feedback transistors to prevent destructive charge leakage (Fig. 7a). While the weak feedback transistors improve the robustness of the flip-flops, they also automatically reset the flip-flops after its internal nodes have been left floating, thus limiting the integration time to 100μs or less. This is fine for this test chip, as the integration time is on the order of 1μs and increased only for pixel characterization.

The final specifications of the image sensor are shown in Table I. The power consumption of the entire chip (including I/O pads) is 20mW. The breakdown of the power is shown in Fig. 10. Total power consumption of the ADCs is 2.6mW which corresponds to 1.9μW per column. The row addressing circuits including the buffers consume 0.73μW per row, whereas the column shift registers dissipate 2.3μW per column. The impact of clock power reduction is expected to become significant in gigajot QIS devices. The ADCs working in tandem with digital circuits consume an average power of 6.4mW.

We define an energy/bit figure of merit for a QIS:

$$FOM = \frac{ADC\ power}{\#\ of\ pixels\ \times fps\ \times N} \quad \left[\frac{J}{b}\right] \qquad (1)$$

where N=1 for single-bit QIS and larger for multi-bit QIS, and which for algorithmic converters is the number of comparator strobes per conversion. It should be noted that this FOM is different from an energy per conversion-step FOM that divides by 2^N, often used in image sensors, thereby reducing the FOM by perhaps 1000x. It is also noted that in the QIS, input offset at 3σ must be less than $1/2V_{LSB}$ (= 0.5mV for this chip) which requires additional power dissipation that is included in our FOM. The FOM of the pathfinder chip is 2.5pJ/b.

TABLE I
SPECIFICATIONS OF THE 1MP BINARY IMAGE SENSOR.

Process		X-FAB, 0.18 μm, 6M1P (non-standard implants)
VDD		1.3 V (Analog and Digital), 1.8 V (Array), 3 V (I/O pads)
Pixel type		3T-APS
Pixel pitch		3.6 μm
Photo-detector		Partially pinned photodiode
Conversion gain		119 μV/e-
Array		1376 (H) X 768 (V)
Column noise		2 e-
Field rate		1000 fps
ADC sampling rate		768 KSa/s
ADC resolution		1 bit (V_{LSB} = 1 mV)
Output data rate		32 (output pins) X 33 Mb/s = 1 Gb/s
Package		PGA with 256 pins
Power	Pixel array	8.6 mW
	ADCs	2.6 mW
	Addressing	3.8 mW
	I/O pads	5 mW
	Total	20 mW

Fig. 11a shows one frame of bits that was measured from the sensor using a back-illuminated transparency printed by inkjet. The magnified image in Fig. 11b shows roughness in the edges of characters. This is likely caused by the resolution (600dpi) of the printer used to print the word "IEEE", leading to a less distinct edge, as seen in the front illuminated microscope photo of Fig 11c. The change in illumination causes an apparent change in the width of the characters. An annotated die microphotograph is shown in Fig. 12.

VII. CONCLUSION

A pathfinder 1MP, 1000fps, single-bit quanta image sensor was designed and tested. The primary focus was to test the feasibility of designing low-power and high-speed readout circuits for a gigajot QIS realization. By taking advantage of a charge transfer amplification technique in the sense-amplifier circuits, and incorporating pseudo-static clock gating units in the row and column circuits, the average power consumption of the entire imager (including the I/Os) is 20mW. The power reduction circuit strategies proven in the pathfinder chip allow us to proceed with confidence to gigajot single-bit QIS implementations in advanced processes. The QIS energy FOM of 2.5pJ/b scaled down with smaller parasitic capacitances and rail voltages in advanced technology nodes suggests power dissipation (including timing and control circuits and pad drivers) in the sub-Watt-level range for gigajot QIS devices, sufficiently low for commercial purposes.

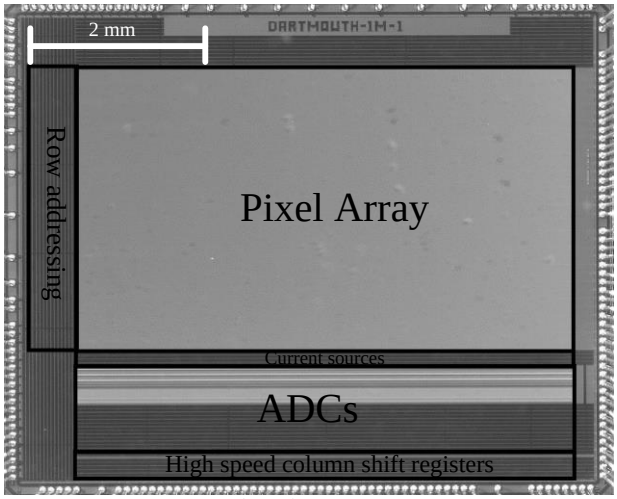

Fig. 12. Micrograph of pathfinder sensor in 0.18 µm CMOS.

ACKNOWLEDGMENT

The authors appreciate the sponsorship and collaboration of Rambus, and the in-kind support and collaboration of X-FAB. The technical advice of Forza Silicon, particularly by B. Mansoorian, D. Van Blerkom, and R. Yassine, in the design review of this sensor is especially appreciated.

REFERENCES

[1] E.R. Fossum, "What to do with sub-diffraction limit (SDL) pixels? - a proposal for a gigapixel digital film sensor (DFS)," in *IEEE Workshop on CCDs and Adv. Image Sensors*, Karuizawa, Japan, June 2005.
[2] E.R. Fossum, "The quanta image sensor (QIS): concepts and challenges," in *Proc. OSA Topical Mtg. on Computational Optical Sensing and Imaging*, Toronto, Canada, July 2011.
[3] E.R. Fossum, "Modeling the performance of single-bit and multi-bit quanta image sensors," *IEEE J. of the Electron Devices Soc.*, vol. 1, no. 9, pp. 166-174, Sep. 2013.
[4] N.A.W. Dutton, *et al.*, "320x240 oversampled digital single photon counting image sensor," in *Symp. on VLSI Circuits*, Hawaii, USA, 2014.
[5] F. Yang, *et al.*, "On pixel detection threshold in the gigavision camera," in *Proc. SPIE. 7537, Digital Photography VI, 75370G*, 2010.
[6] A. Stern, *et al.*, "Digital photon-counting geiger-mode avalanche photodiode solid-state monolithic intensity imaging focal-plane with scalable readout circuitry", U.S. Patent 7 858 917 B2, Dec. 28, 2010.
[7] S. Masoodian, *et al.*, "Early research progress on quanta image sensors," in *Proc. Int. Image Sensor Workshop*, Utah, USA, June 2013.
[8] E. R. Fossum, *et al.*, "High sensitivity image sensors including a single electron field effect transistor and methods of operating the same", U.S. Patent 8,546,901, Oct. 1, 2013.
[9] J. Ma, *et al.*, "Jot devices and the quanta image sensor," in *Proc. of the IEEE Int. Electron Devices Mtg. (IEDM)*, San Francisco, CA, 2014.
[10] J. Ma, and E.R. Fossum, "A pump-gate jot device with high conversion gain for a quanta image sensor," *J. of the Electron Devices Soc.*, vol. 3, no. 2, pp. 73-77, 2015.
[11] E. R. Fossum, "Investigation of two-layer photodetectors for YSNR10 improvement in submicron pixels," in *Proc. Int. Image Sensor Workshop*, Hokkaido, Japan, 2011.
[12] S.T. Koshinen, *et al.*, "Color filters for sub-diffraction limit-sized light sensors", U.S. Patent 8 134 115 B2, Mar. 13, 2012.
[13] L. Anzagira and E. R. Fossum, "Color filter array patterns for small-pixel image sensors with substantial cross talk," *J. Opt. Soc. Am. A*, vol. 32, no. 1, pp. 28-34, 2015.
[14] T. H. Lee, *et al.*, "Partially pinned photodiode for solid-state image sensors, " U.S. Patent 5 903 021, Jan. 1997.
[15] K. Kotani, *et al.*, "CMOS charge-transfer preamplifier for offset-fluctuation cancellation in low-power A/D converters," *IEEE J. Solid-State Circuits*, vol. 33, no. 5, pp. 762-769, May 1998.
[16] W. J. Marble, et al., "Analysis of the dynamic behavior of a charge transfer amplifier," IEEE *Trans. Circuit and System-I*, vol. 48, no. 7, July 2001.
[17] S. Masoodian, *et al.*, "Low-power readout circuit for quanta image sensors," *Electronic Letters*, vol. 50, no. 8, pp. 589-591, 2014.
[18] C.Yeh, and Y. Lai, "Low power readout control circuit for high resolution CMOS image sensor," in *Proc. ISCAS*, pp. 1163-1166, 21-24 May, 2006.
[19] [Online]. Available: http://edt.com/product/pcie4-cda/.
[20] [Online]. Available: www.digilentinc.com/atlys/.

Saleh Masoodian (S'08) received a B.S and M.S. degrees in electronic engineering from University of Tehran, Tehran, Iran, and Ferdowsi University of Mashhad, Mashhad, Iran, in 2009 and 2012, respectively. He is currently pursuing a Ph.D. degree at Thayer School of Engineering, Dartmouth College, Hanover, NH, USA. His current research is focused on realizing quanta image sensor (QIS) technology by designing low-power and high speed readout circuits.

Arun Rao (S'14) is currently a Ph.D candidate at Thayer school of Engineering at Dartmouth. He completed his B.E (EE) from Bangalore University in 2005, and MS (EE) from Utah State University in 2010. His primary interests are in the field of low-power analog, mixed-signal IC design. He is working on novel circuits for image sensors and implantable biomedical devices.

Jiaju Ma (S'12) was born in China. He received the B.S. degree in applied physics from Nankai University, Tianjin, China, in 2012. He is currently pursuing the Ph.D. degree from the Thayer School of Engineering, Dartmouth College, Hanover, NH, USA, researching the fabrication and operation of CMOS image sensors with a particular emphasis on the jot device TCAD modeling and fabrication process for Quanta Image Sensors.

Kofi Odame (S'06–M'08) received the B.Sc. and the M.Sc. degrees in electrical engineering from Cornell University, Ithaca, NY, USA, and the Ph.D. degree from the Georgia Institute of Technology, Atlanta, GA, USA, in 2002, 2004, and 2008, respectively. Currently, he is an Assistant Professor of electrical engineering at the Thayer School of Engineering, Dartmouth College, Hanover, NH, USA. His interest is in analog integrated circuits for nonlinear signal processing.

Eric R. Fossum (S'80–M'84–SM'91–F'98) is currently a Professor with the Thayer School of Engineering at Dartmouth. He is the primary inventor of the CMOS image sensor used in billions of camera phones and other applications. He was inducted into the National Inventors Hall of Fame and is a member of the National Academy of Engineering. He is co-founder and Past President of the International Image Sensor Society. He is currently exploring the Quanta Image Sensor.