TCAD Modeling of Devices for Quanta Image Sensors

Jiaju Ma and Eric R. Fossum

1 April 2015
Review of CMOS Image Sensor with a pinned photodiode
Review of CMOS Image Sensor with a pinned photodiode
Review of CMOS Image Sensor with a pinned photodiode
Review of CMOS Image Sensor with a pinned photodiode
Review of CMOS Image Sensor with a pinned photodiode
Review of CMOS Image Sensor with a pinned photodiode

\[ dV = \frac{dQ}{C} \]
Review of CMOS Image Sensor with a pinned photodiode

One 4T Pixel
The goal for QIS is to make a very tiny, specialized pixel (“jot”) which could sense a single photo-electron and output binary data.

Jots array would be readout by scanning at a high frame rate to avoid likelihood of multiple hits in the same jot and loss of accurate counting.

Image pixels could be created by combining jot data over a local spatial and temporal region using image processing.
Quanta Image Sensor (QIS) Motivation

- Photons are digital in nature according to particle view of light and can be represented by binary data.
- Better images can be obtained by oversampling in time and space.
- More applications, such as motion blur correction.
Jot Device Concept

Specialized *tiny* pixel, sensing *single* photo-electron, output *binary* data

<table>
<thead>
<tr>
<th></th>
<th>Jot</th>
<th>Pixel</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>650nm (10L)</td>
<td>1.1um*(17L)</td>
</tr>
<tr>
<td>Storage Capacity</td>
<td>1-100e-</td>
<td>~10000e-</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>&gt;1mV/e-</td>
<td>100uV/e-</td>
</tr>
<tr>
<td>Read Noise</td>
<td>0.15e- rms</td>
<td>~2e- rms</td>
</tr>
</tbody>
</table>

*65nm CMOS CIS process*
Jot Device Design

Shrink size
Jot Device Design

**Improve sensitivity**

\[ dV = \frac{dQ}{C_{FD}} \]

\[ C.G. = \frac{dV}{dQ} = \frac{1}{C_{FD}} \]

\[ C_{FD} = C_j + C_{ovtg} + C_{ovrg} + C_{sf} + C_{metal} \]

*1.4\text{um} PPD Pixel

\[ CFD=1.55fF \]

\[ C.G.=103uV/e^- \]
Pump gate charge transfer
Pump gate charge transfer
Tape-out chip with 65nm CIS process

- Jot with pump gate TG 1.4um, FWC=200e-
- Jot with pump gate TG and tapered RG 1.4um, FWC=200e-
- Jot with pump gate TG and 4-way shared readout 1 um, FWC=200e-
Tape-out chip with 65nm CIS process

**Baseline PPD pixel**
- $C.G. = 103\mu V/e$

**Pump gate JOT**
- $C.G. = 238\mu V/e$

**Tapered RG+ smaller SF**
- $C.G. = 380\mu V/e$

**4-way shared JOT**
- $C.G. = 212\mu V/e$

Diagram showing capacitance values for different components:
- FD junction cap
- TG overlap cap
- RG overlap cap
- SF cap
- Metal cap
Gate-less Reset

Reduce capacitance, reduce column wires

Reduce capacitance, reduce column wires

\[ TG \quad \text{n} \quad \text{p} \quad RG \quad \text{n} \quad \text{p} + \]

\[ TG \quad \text{n} \quad \text{p} \quad Vrst\_low \quad Vrst\_high \]
Gate-less reset

$V_{rst\_high} = 5V$

$V_{rst\_low} = 2.5V$

$V_{pulse}$

FD

RD

Potential (V)

Before RST ($V_{rd} = 2.5V$)

During RST ($V_{rd} = 5V$)

After RST ($V_{rd} = 2.5V$)
JFET source follower with FD being the virtual gate

Reduce capacitance, reduce readout noise
JFET source follower with FD being the virtual gate
JFET source follower with FD being the virtual gate.
# Jot device summary

<table>
<thead>
<tr>
<th></th>
<th>Jot</th>
<th>Target</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size</td>
<td>800nm (12L)</td>
<td>650nm*</td>
</tr>
<tr>
<td>Storage Capacity</td>
<td>100e-</td>
<td>1-100e-</td>
</tr>
<tr>
<td>Conversion Gain</td>
<td>1.7mV/e-</td>
<td>&gt;1mV/e-</td>
</tr>
<tr>
<td>Read Noise</td>
<td>Waiting for test results</td>
<td>0.15e- rms</td>
</tr>
</tbody>
</table>

*65nm CIS process*
Reference


Thanks for your attention!