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Jot Devices and the Quanta Image Sensor

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Abstract

The Quanta Image Sensor (QIS) concept and recent work on its associated jot device are discussed. A bipolar jot and a pump-gate jot are described. Both have been modelled in TCAD. As simulated, the pump-gate jot has a full well of 200e- and conversion gain of 480uV/e-.

Introduction:

The Quanta Image Sensor (QIS) is a possible third generation solid-state image sensor concept that seeks to take advantage of shrinking pixel sizes. Pixel shrink, good for smaller cameras or larger format sensors, normally suffers from diminishing full well capacity and concomitant SNR and image quality deterioration. The QIS represents a different paradigm in image capture where small full well is overcome by digital integration with faster readout, and power dissipation offset by reduced ADC bit depth (1). The ultimate single-bit QIS has an effective full well of one electron and a single-bit ADC.

The commercial realization of the QIS requires overcoming many significant technical challenges. It is an oversampled image sensor in both space and time, using both sub-diffraction limit (SDL) pixel sizes (e.g. <900nm) and very high field rates (e.g. 1000fps). In addition to the SDL pitch, the photodetectors have small full-well capacity, typically less than 200e-, and high conversion gain (e.g., 1mV/e-) so that each photoelectron can be counted with low bit-error rate. In the single-bit QIS, each output is binary in nature and an output image pixel is composed from many such SDL photoelement outputs across bit planes from several (e.g., 16) fields as illustrated in Fig. 1. Thus photoelements are given a special name, "jot", meaning smallest thing. The QIS is intended to have of the order of 0.1-10.0 Gjots leading to output data rates of 0.1-10 Tb/s.

The potential advantages of the QIS over current CMOS image sensors include low-light sensitivity, adjustable tradeoff in resolution vs. sensitivity even after image capture, noiseless time-delay and integration (TDI) along an arbitrary track, also after image capture, and a film-like

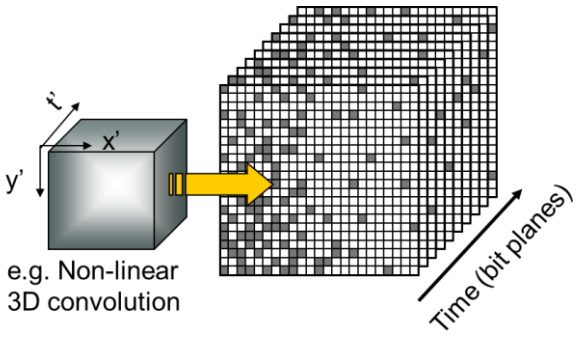


Figure 1. Conceptual schematic for creating pixels from QIS jots.

D-log(H) exposure characteristic that yields intrinsic overexposure latitude as shown in Fig. 2 (2). Signal, noise and exposure-referred SNR (SNRH) is shown in Fig. 3 for an example summation of a 16x16x16 (X,Y, t) "cubicle" of jots, used to create a single pixel. Combining fields with different shutter settings allows high dynamic range without sudden SNR dips. By moving the digital domain right up against photoelectron capture, the process of image formation is altered from having a physically defined pixel on the sensor, to permitting flexible, programmable pixel creation in the digital domain following signal capture.

The small jot size and the fast field-readout rate is more about what we term "flux capacity" than about spatial or

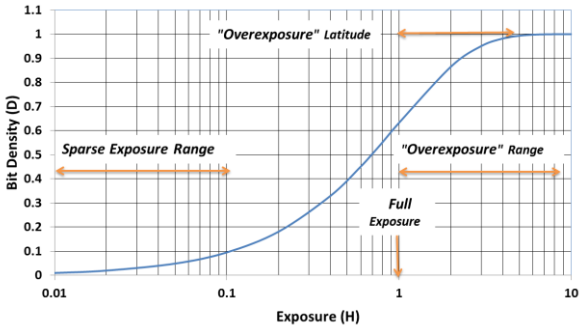


Figure 2. Bit density vs. exposure for QIS showing D-log(H) film-like characteristic. Bit density is effectively the probability that a jot has captured a photoelectron for a given quanta exposure H.

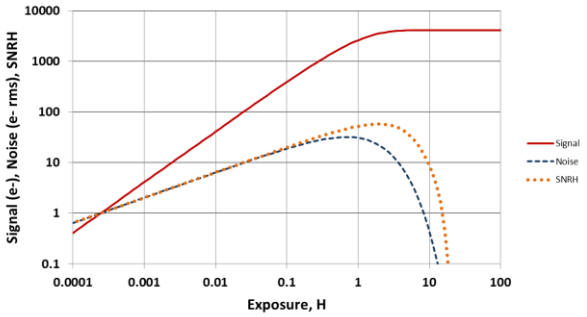


Figure 3. Signal, noise, and exposure-referred SNR as a function of exposure H for an (X,Y,t) cubicle of 16x16x16 = 4096 jots.

temporal resolution in the QIS, although higher resolution comes along as part of the nature of the device. The nominal "full well" photon flux ϕ_{wn} that can be handled by the QIS can be written as

$$\phi_{wn} = jf_r(2^n - 1)/\sigma\bar{\gamma} \qquad (1)$$

where j is the jot density, f_r is the field readout rate, n is the ADC bit depth (n=1 for single-bit QIS), σ is the electronic shutter duty cycle, and $\bar{\gamma}$ is the average conversion efficiency of incident photons to collected photoelectrons. For consumer applications, the flux capacity of the QIS should be similar to that of CMOS image sensors and this drives high values for jf_r. Multi-bit QIS devices are also being considered for increasing flux capacity, with $1 < n \lesssim 6$. Very bright light and flash photography remain possible issues. For other applications, such as low-light vision, the jot density can be relaxed.

Readout of the QIS is architecturally similar to that of conventional CMOS image sensors, with column-parallel readout consisting of sense amplifier and ADC. We have recently reported some readout circuit progress (3). We have since demonstrated about 5pJ/b for the sense amp and 1b ADC in a 1Mpix binary sensor with 3.6um pixel pitch operating at 1000fps (1Gb/s) in 0.18um CMOS that will be reported separately. Realization of a consumer gigajot sensor requires an order of magnitude reduction in energy/bit that will be accomplished by supply rail scaling, technology node scaling, and improved circuit design. It is expected that a gigajot sensor (e.g., 42k x 24k) would be best implemented in a sub-65nm process with $\lesssim$500nm jot pitch.

We have been making steady progress on several fronts – low-power bit-plane readout, the jot device itself, algorithms for output image creation, and understanding the general imaging characteristics of the QIS. In the remainder of this paper, we will concentrate on the electron device element at the heart of the QIS, the jot device.

Jot Devices

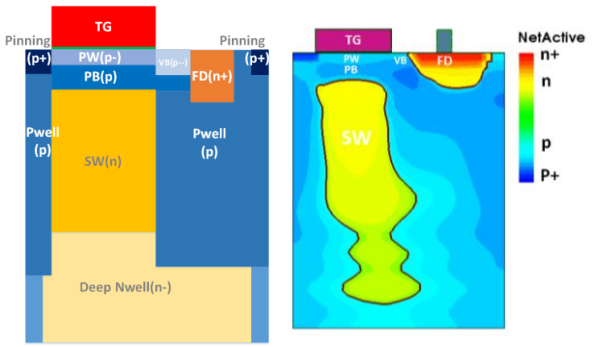
The jot device has many requirements in common with a modern CMOS image sensor (CIS) pixel. It must have high quantum efficiency (including fill factor), good photoelectron collection efficiency, and low dark current. In addition, it must have low readout noise and essentially no lag. Readout noise in state-of-the-art (SOA) CIS is of the order 100-200uV r.m.s. yielding input-referred read noise of a few electrons r.m.s. To get above the read noise for a single photoelectron, one needs at least 200uV/e- conversion gain, and for low bit-error rate (one photoelectron is one bit in the QIS) the read noise must be below about 0.15e- rms (2) suggesting a conversion gain of about 1mV/e- (0.16fF). This is perhaps 5x higher conversion gain than found in SOA CIS devices. However, compared to CIS devices, the full-well capacity (FWC) requirement is greatly relaxed (e.g., from at least 3000e- to less than 200e-). FWC is a major difficulty for CIS pixel shrink today and one of the motivating factors for exploring the QIS paradigm. Crosstalk between adjacent jots of the same color is not as critical as in SOA CIS because we are already below SDL pitch. Several jots may be under a single color filter and microlens.

In our work we consider only backside-illuminated (BSI) devices. Four basic approaches have been considered thus far. First is shrinking SPAD devices to SDL pitches. This seems a more distant horizon at this time. However, a low-density SPAD-based-jot QIS has been recently demonstrated with 77kjots with 8um pitch in 0.13um CMOS operating at 5000fps (4). Second is the use of a single-electron FET detector (5) that due to IP reasons we are not currently pursuing but remains interesting.

At Dartmouth, we have considered a bipolar-based jot and a pump-gate jot. Both start from structures similar to those used in modern CIS pixels. Adapting technology developed for CIS pixels is sensible in creating the QIS jots, speeding development and reducing barriers for adoption. A pump-gate jot has been designed in a modified 65nm CIS process and is being fabricated. The 1.4um pitch was determined by preexisting circuits and could be readily reduced in the future.

Pump-Gate Jot

The pump-gate jot is similar CIS pixels with several differences. First, the carriers are stored under the transfer gate (TG) to reduce jot area. Second, the floating diffusion (FD) is moved distally from TG to reduce overlap capacitance. Third, a tapered reset gate is proposed to further reduce overlap capacitance. Fourth, complete transfer of charge takes two steps: (a) a vertical transfer



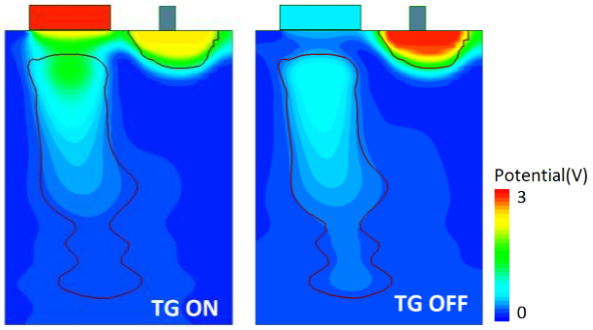
(a) (b)

Figure 4. Schematic of (a) pump gate jot doping and (b) TCAD simulation.

upwards to surface under TG, followed by (b) a lateral transfer over the "virtual phase" barrier (VB) between TG and FD. The two steps constitute the "pump" action of the charge transfer – similar to a technique used in two-phase CCDs (6) and more recently in a global-shutter CIS (7).

Some recent reported CIS pixels have included storage under the transfer gate (8,9) but since high capacity is needed, implementation has been their major challenge. The small full-well capacity of a QIS jot makes it possible to shrink the size of the device compared to CIS pixels. In the proposed BSI device, a shallow buried-photodiode storage well (SW) is formed underneath the transfer gate, surrounded by a p-type doped well. As depicted in Fig. 4, an n-type SW photodiode well is formed below TG. On the top of SW, there are two p-type doped regions PB and PW, and PW is more lightly doped than PB, so that when TG is biased by flat band voltage, the potential of PW is higher than PB. Between PW and FD, is the p-type doped "virtual-phase" potential barrier (VB). It is more lightly doped than PW. Together they form a double-step potential profile. The p+ pinning layer on the side of TG helps quench surface-generated dark current.

The potential profile is shown in Fig. 5 for the cases of TG



(a) (b)

Figure 5. Potential in pump-gate jot for (a) TG ON and (b) TG OFF

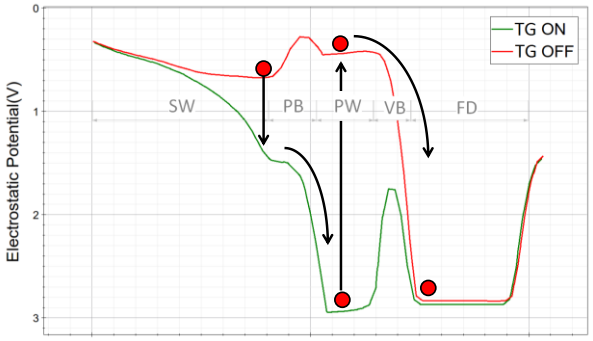


Figure 6. Potential along transferred photoelectron path.

On and Off. During integration TG is "Off" and photoelectrons are collected in SW. After integration, TG is positively biased (On), and carriers are transferred from SW to PW. This is the first step of the "pump" action charge transfer. VB is in depletion mode and forms a virtual barrier between PW and FD. When TG is turned off, the potential of PW returns to its initial level, and as soon as the potential of PW becomes lower than VB, charge in PW will flow over VB into the distal FD. Meanwhile, because of the doping concentration and the location, PB always has a lower potential than PW, which prevent charge from flowing back to SW. This is shown in Fig. 6. Thus, by double step "pump" action, complete charge transfer can be achieved with low TG overlap capacitance.

A complete 1.4um pump-gate jot design with distal FD and other layout improvements such as tapered reset gate is estimated to achieve 480uV/e- with 200e- full well. The distal FD design also reduces clock feedthrough to the column bus when TG is pulsed.

Additional jot-area savings comes from shared readout as is commonly used in CIS pixels. 4-way shared readout was implemented with a 1.0um jot pitch. With the distal FD, the additional TG gates will not increase FD capacitance due to overlap, but 4-way sharing has lower conversion gain of 250uV/e- due to FD size and the remote reset gate. Using

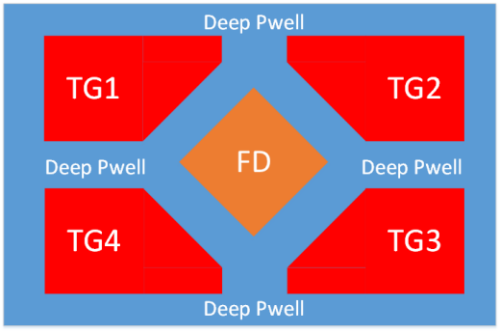


Figure 7. Four-way shared pump-gate jot floorplan, not including reset, selection and SF transistors.

the same baseline process and simulation, a conventional 4-way shared CIS pixel has a conversion gain of 70uV/e-.

The four jots could be covered by a single color filter and micro lens. Such a microlens might be implemented with a center dimple to avoid guiding rays to the FD. With SDL jots, it is not critical which of the four adjacent jots photoelectrons randomly enter, provided that they are not lost to FD. A deep p-well will be used surrounding four adjacent jots for isolation and photoelectron deflection from FD. An example of a 4-way shared-readout jot floor plan is shown in Fig. 7.

Both the 1.4um jot with non-shared readout, and the 4-way shared-readout 1.0um jot, are currently being fabricated.

Bipolar Jot

A PNP bipolar jot device was also explored as shown in Fig. 8. As a starting point, the pinning layer of pinned photodiode (PPD) was configured as an emitter, and the storage well as the base, and the substrate and a collector common to all jots. The CIS pixel reset gate was used to reset the base so that all majority carriers are depleted.

The main idea is that a single photoelectron collected into the fully depleted base causes the base potential to shift, according to the capacitance of the base. By using an emitter-follower readout circuit configuration, the base-emitter capacitance contributes little to the base capacitance. The base voltage change is transferred to the column bus where it can be sensed. The conversion gain for the jot is determined by the base capacitance in emitter-follower configuration.

In fact, the emitter-collector hole current wants to flow through the base at point of minimal base potential, whereas the photoelectrons want to gather at a point of maximum base potential. Thus, a confinement of the photoelectron at a point of minimum base width is needed to modulate hole current. A collar structure was created to implement the confinement, and some modulation of the base voltage was observed in simulation. It was also found that collecting photoelectrons modulated the effective base width. However, satisfactory operation of the bipolar jot was not obtained in simulation and we are focusing on the pump-gate jot.

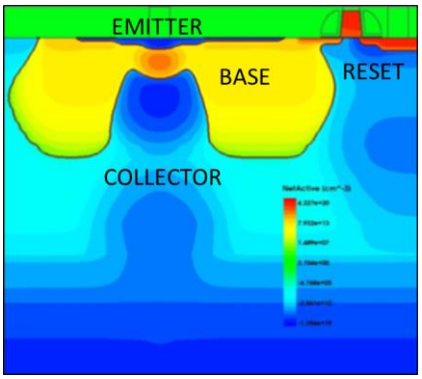


Figure 8. Bipolar jot doping

Conclusions

The Quanta Image Sensor has been described and two approaches for jot implementation have been discussed. The pump-gate jot, implementing by modifying a conventional BSI CIS pixel, was simulated and implemented. We are awaiting experimental devices.

Acknowledgments

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