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The Quanta Image Sensor (QIS): Concepts and Challenges

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Abstract: The Quanta Image Sensor (QIS) concept is presented and its novel properties discussed. Approaches and challenges to counting photoelectrons and Tbit/s readout are discussed. (Invited).
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1. Introduction

In counting every photoelectron, the Quanta Image Sensor (QIS) represents a paradigm shift in imaging. Historically, solid-state image sensors such as the charge-coupled device (CCD) and the CMOS active pixel sensor (APS) are organized as photoelectron "buckets" or pixels that both collect and integrate photogenerated carriers in the semiconductor. The signal handling capacity of the bucket, measured in electrons, is the full-well metric and it determines the dynamic range and maximum SNR in an image. Pixel pitch in consumer image sensors has shrunk to the 1400-1100 nm range, typically below the diffraction limit of the imaging system. A next generation at 900 nm pitch is expected [1]. Shrinking the pixel creates many problems. Perhaps the most important is deterioration of the YSNR10 metric [2] which is due to fewer photoelectrons. Dynamic range also suffers due to reduced full-well capacity. In color sensors, color crosstalk is also an issue. While pixel shrink can improve camera size, weight and cost, optical diffraction places a limit on resolution improvement. Among consumer image-sensor suppliers, pixel shrink constitutes a major R&D effort and cost. A good example is the adoption of backside illumination (BSI) for mass production [3] which gained about one generation in pixel shrink at substantial expense.

With the QIS, aspects of the pixel-shrink race are replaced with other technological challenges. Implementation of the QIS will allow new imaging capabilities for many applications; whether these new capabilities will prove to be a compelling advantage for consumer use is yet to be seen.

2. QIS and Image Formation Concept

The QIS consists of an array of billions of nanoscale, binary active pixels – referred to as "jots" from the Greek for smallest thing. Each jot has binary output representing the absence ("0") or presence ("1") of a photoelectron. The array of jots is scanned at a high rate as a bit plane. Generally, the bit plane will be sparsely populated except when imaging near saturation conditions. A block diagram is shown in Fig. 1.

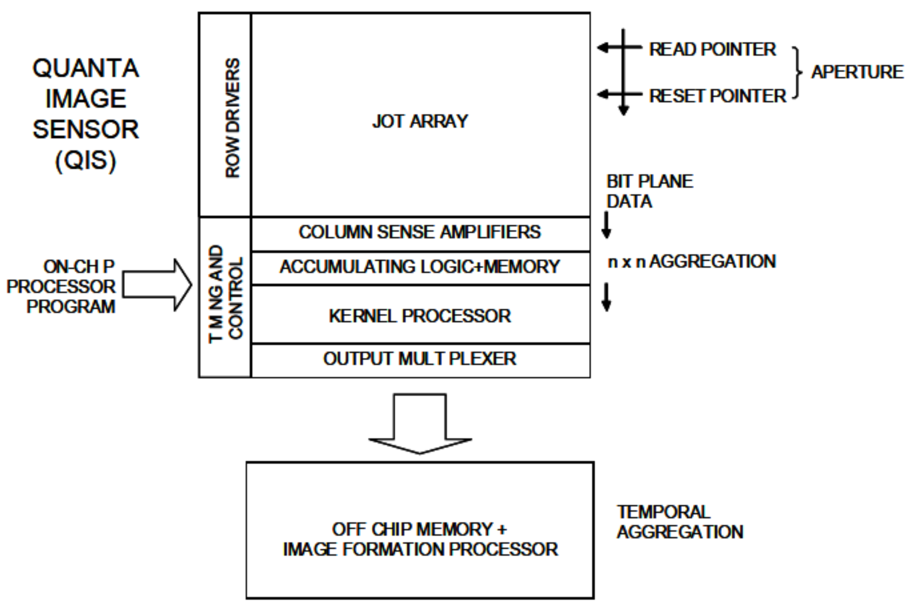

Fig. 1. Schematic illustration of possible floorplan and and data flow. Note that for higher throughput, sense amplifiers can also be placed at the top of the jot array, and row driving would be performed from both sides of the array.

The Gbit-plane of data is read into digital memory where it is digitally integrated over 10-100 subframes. Digital integration using external memory is a fundamental change from the way imaging is typically performed. In the QIS, subsequent sub-frames may be shifted or morphed prior to integration to allow functions such as motion compensation, TDI (in arbitrary track direction) and wavefront correction. Depending on the application, multiple sub-frames may be stored prior to shift and integration to allow motion-flow analysis to be performed. A billion jots at 1,000 scans/s leads to Tbit/s data rates. Getting this data off the sensor and into memory may be difficult in the near future so that some aggregation of data in the image sensor may be required.

In the QIS, image formation congruent with current imaging technology would involve digital integration of bit-planes over a spatial extent corresponding to a conventional pixel (e.g. 14x14 jots) and in time (e.g. 15 jots) – sort of a bit cube formed from 2,940 jots samples. The pixel formed by the image formation processor would have a full-well equivalent of 2,940 electrons.

We can compare corresponding metrics in a conventional sensor to the QIS. Consider a 3,264x2,448 (8 Mpixel) conventional CMOS APS image sensor with 1400 nm pixel pitch. Its full well is about 3,000 electrons, the same as the QIS example. Frame rate is 15 Hz corresponding to a column scan rate of 40 kHz and output data rate of 120 Mpixel/s. The corresponding QIS jot pitch would need to be 100 nm with sensor scan rate of about 225 Hz and column scan rate of 8MHz. The output data rate would need to be approximately 0.4 Tbit/s without on-chip aggregation.

In the case that the jot pitch is increased from 100 nm to 200 nm in the same comparative example, the photon hit-rate per jot increases due to the increased jot area. The column scan rate must be increased to 64 MHz and the sensor scan rate to 900 Hz yielding the same output data rate of 0.4 Tbit/s. This is because the output data rate corresponds to the total photoelectron generation rate in either the QIS or conventional sensor under saturation conditions. It is an interesting feature of the QIS that the sensor scan rate decreases inversely with increasing jot density.

Many scanning and rolling shutter techniques developed for CMOS image sensors are applicable to QIS devices. In addition, since multiple scans are required to create a single image, the scans need not be periodic. Aperiodic scans (scans with variable dwell times between scans) can be used to reduce power and output data rate.

Like conventional CMOS image sensors, a rolling shutter can be used to reset rows of jots at a preset time before readout. This can reduce the temporal aperture from one full scan cycle down to a single row time (e.g. from perhaps 4 msec to 33 nsec or about 100,000x reduction in aperture) This is useful when the photocarrier generation rate in a jot exceeds the scan rate of the QIS.

High dynamic range (HDR) imaging can be achieved in CMOS image sensors by taking successive scans at different rolling shutter apertures [4, 5]. For example, one exposure can be taken at wide-open condition, and one at minimum aperture. The long exposure and short exposure images are then fused using some technique (for example, simply adding the images) leading to either linear or non-linear photon transfer characteristics. In QIS device, many more scans are already taken per image frame so the opportunity for HDR imaging is substantially increased. Non-linear transfer characteristics are sometimes useful when considering that full bit counts become unnecessary in the presence of shot noise.

Image formation in the QIS can be quite different from conventional image sensors. In conventional image sensor emulation, "hits" within rigid, non-overlapping pixel boundaries of space and time are weighted by unity, and those outside ignored. In the QIS, we can convolve bit-cubes with arbitrary weighting functions. For example, bits centered in the cube can be weighted higher than those at the periphery, and a weighting function tail can extend beyond the nominal pixel limits in both space and time. The weighting function can be adaptively adjusted to achieve imaging performance objectives. See Fig. 2.

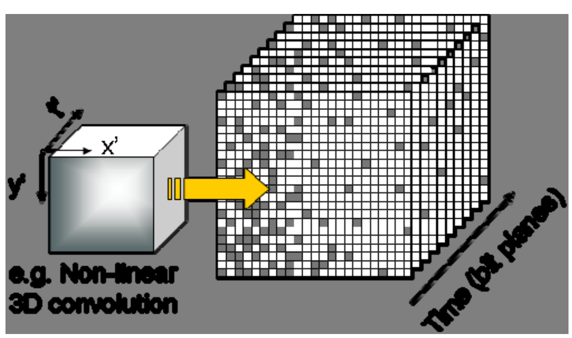

Fig. 2. Illustration of spatio-temporal convolution with QIS bit-plane data

Another type of image formation process is to emulate digital film [6]. In this process a single "hit" within some arbitrarily defined grain boundary results in all bits flipping within the grain. Like film, the larger the grain, the more sensitive the sensor is to light with consequent reduction in resolution. Also like film, such a sensor will exhibit D log H exposure characteristics, of interest to photographers and other wide dynamic range imaging applications. The grain size can be selected *a posteriori* to optimize imaging characteristics.

3. Challenges

Nearly every aspect of the QIS represents a technological challenge. First and foremost is implementation of the jot itself. It must collect the photoelectron and have enough gain and low enough noise to produce a low bit-error-rate (BER) signal on a column readout bus. It is estimated that the signal needs to be approximately 10 mV and the noise less than 0.1 e- rms. At least, two candidate approaches can be considered – single photon avalanche detectors (SPAD) [7,8] and single electron field effect transistor (SEFET) [9]. Brute force scaling of the CMOS APS device is also possible. Scaling of a CMOS APS pixel to 100-200 nm pitch will be challenging but conceivable.

SPAD devices are realized only in relatively small arrays (32x32) thus far, and SPAD pitch is typically 10,000 nm or more. Great advancement would be required in SPAD technology for it to be applied in the QIS. However, the demonstrated high gain and photon-counting capability of the SPAD is appealing.

The most attractive approach thus far seems to be implementation of a SEFET. In a SEFET, the presence of a single electron on the gate changes the FET current enough so that it can be detected. Thus far, SEFETs have only been modeled using TCAD. TCAD modeling showed greater than 5 mV/e- conversion gain in a source-follower configuration. However, many practical issues still need to be worked out.

It is interesting to note that random telegraph signal (RTS) noise from single-electron-trap charging in the pixel FETs is the dominant noise source in CMOS image sensors today. In essence, we need to change the noise to signal.

A second challenge for QIS implementation is implementation of high-speed, low-power sense amplifiers at the bottom of every column in the QIS. While akin to DRAM sense amplifiers, increased speed and much reduced power is required in the QIS.

Data I/O is another area of challenge for implementing the QIS. Moving Tbit/s off chip with low power is another critical function to be realized. While some on-chip data reduction is possible to make data I/O possible, the full potential of the QIS is realized when all bits can be utilized by the image formation processor.

One of the greatest challenges in the QIS is in the image formation processor. Algorithms for image formation are yet to be created, although related work in so-called "gigavision" cameras has shown progress on this front [10]. Still, many open questions remain such as management of SNR and resolution and their trade off.

4. Conclusion

In the QIS concept, we retain the nature of the discrete photon intensity field and we move image formation from the inflexible semiconductor device level to the very flexible digital domain. Accessibility to such basic image formation processes by image processing specialists will undoubtedly lead to new and interesting imaging paradigm shifts. Much work is needed to realize the full potential of the QIS concept and we are just at the beginning.

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