An 8.3-Megapixel, 10-bit, 60 fps CMOS APS

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This paper discusses a 1¼-inch, 8.3 megapixel, digital-output, monochrome CMOS APS for ultra high definition television (UDTV) applications. The UDTV system requires 8.3 million pixels, 60 fps progressive scan mode operation, and at least 10-bit ADC resolution, translating into an effective data rate of 5.2 Gbps. Image sensors and prototype camera systems for such applications have previously been developed [1]–[3]. However, they required large optical systems and numerous external components and had high power consumption, so their practical use was limited.

The CMOS sensor presented here was fabricated on a 0.25μm process and includes a 3,936H x 2,196V (3,840H x 2,160V effective) pixel array. Its pixel pitch of 4.2μm enables a 1¼-inch optical format while avoiding the use of stitching or alternative techniques, since the die size of the chip fits into the standard 20mm-x-20mm reticle window. The 4.2μm pixel is a 3T n-well/p-substrate photodiode with on-chip microlenses. The drawn fill factor of the pixel is approximately 40 percent. Optical black pixels with metal and black filter material shielding are located at the periphery of the effective pixels to obtain a high-precision black-level reference. A block diagram of the sensor architecture is shown in Figure 1. The pixel rows are read out in parallel through an analog gain stage with gain settings of x0.7, x1.0, x1.2, x2.0, and x4.0. The sampled pixel values from pairs of columns are, in turn, transferred to the column parallel, pair-wise, common ADCs; thus, two ADC conversions occur per row readout time, as indicated in Figure 2. The column and ADC readout chain is illustrated in Figure 3. The ADC outputs are sequentially sampled into a front-end SRAM bank during digitization. When this is completed, the entire row data is transferred in parallel into a second back-end SRAM bank available for readout. The 16-port parallel readout can thus take place serially during conversion of the subsequent pixel row. The analog pixel readout, ADC and SRAM arrays are split into two banks at the top and bottom of the array, each having 984 (960 effective) ADCs. This maximizes the layout pitch available for the column parallel readout. The timing control circuits generate all necessary control signals from four input signals: master clock, frame trigger, row trigger, and shutter trigger.

Design techniques applied to achieve the necessary data rate while ensuring good noise and uniformity performance and high-quality image reproduction are presented. The chosen architecture allowed a high degree of parallel processing for high frame rates and, at the same time, sufficient layout pitch for the analog readout and ADCs. Noise-robust bias circuits were implemented to increase the array uniformity, as illustrated in Figure 4. High power supply rejection in the pixel columns were important due to the potentially high noise levels caused by the readout speed and array size. Fixed-pattern noise (FPN) generated in each pixel and column readout is suppressed before A/D conversion, and a carefully designed analog multiplexing stage minimizes the potential pair-wise FPN introduced by the shared ADC architecture. Potential FPN caused by the offset voltage variations of the ADC comparators is suppressed by self-calibration functionality

implemented in each ADC, as illustrated in Figure 3. The automatic calibration routine is run for every frame to compensate for temperature drifting. Calibration values can also be manually written to and read from the ADCs through a dedicated serial interface. The dual SRAM bank allows row timing as illustrated in Figure 2. Note that the pixel readout, analog gain and sample-and-hold operations take place when the digital data readout is quiet, thus minimizing the coupling noise. The back-end SRAM bank is read out differentially using on-chip sense-amps to output a digital data stream.

A reproduced image obtained from the 8.3-megapixel UDTV sensor operating at 60 fps with a column gain of x1.0 is shown in Figure 5. A magnified image from the center portion resolving 2,000 TV lines is shown in Figure 6.

Power consumption is less than 760mW, including output driving at 60 fps progressive-scan mode with a 49.5 MHz master clock and 3.3V supply. Conversion gain is 0.06 LSB/e-, corresponding to 43 μV/e- at the photodiode. Saturation charge and random noise are 25,000e- and 42e-$_{r.m.s.}$ (2.5 LSBs) respectively, with an ADC input range of 750mV, analog gain of x0.7 and hard reset operation. This yields a dynamic range of 55.0dB. The pixel-reset noise component is estimated to be 35e-$_{r.m.s.}$, suggesting the random noise to be dominated by this noise factor. FPN including the FPN caused by the column parallel processing is less than the random noise level and measured to <1.2LSB at gain x1.0. Sensitivity with on-chip microlens was measured to be 4.2 kb/lux-sec (3.0 V/lux-sec) using a 2,700K light source and an IR-cut filter with a cut-off wavelength of 650nm.

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References

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Figure 1 Sensor Architecture

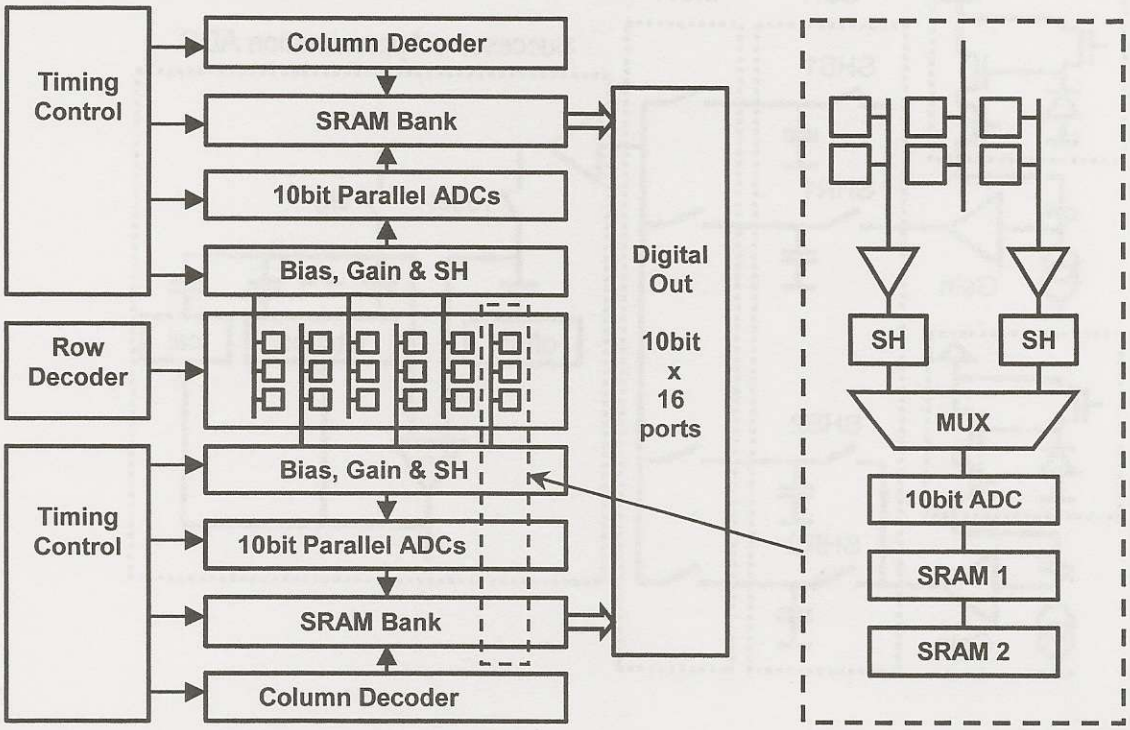

Figure 2 Row Operation Timing

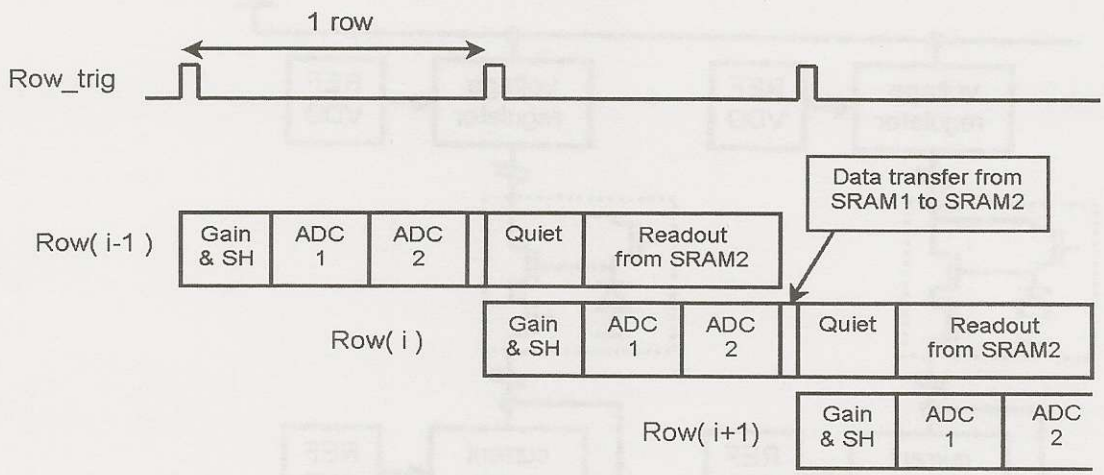

Figure 3 Column and ADC Signal Chain

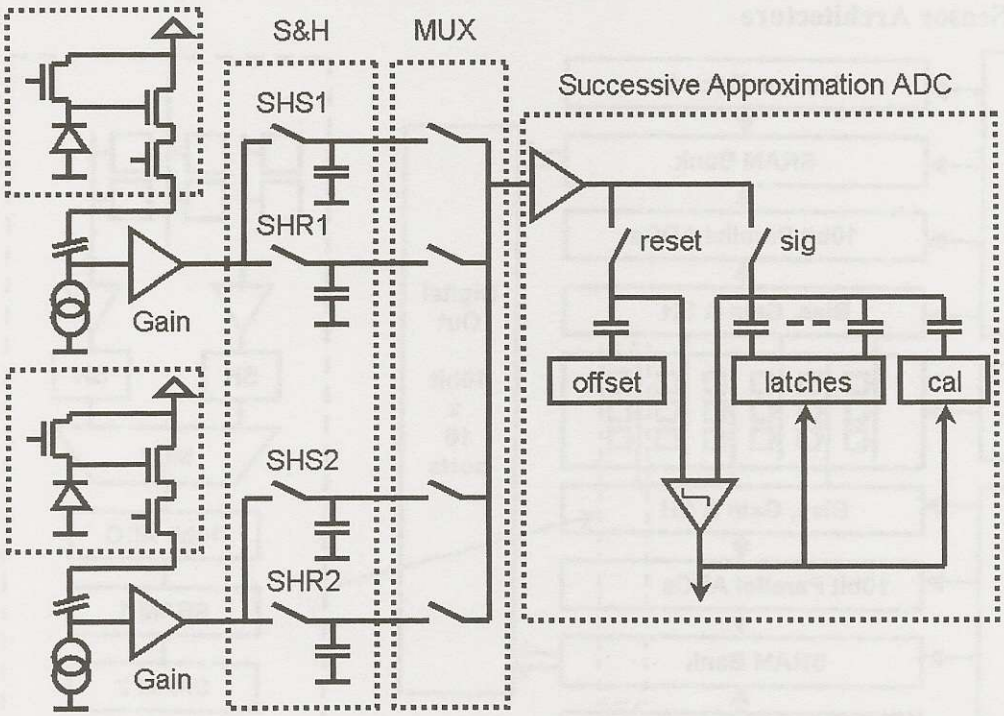

Figure 4 Pixel Column Bias Circuit

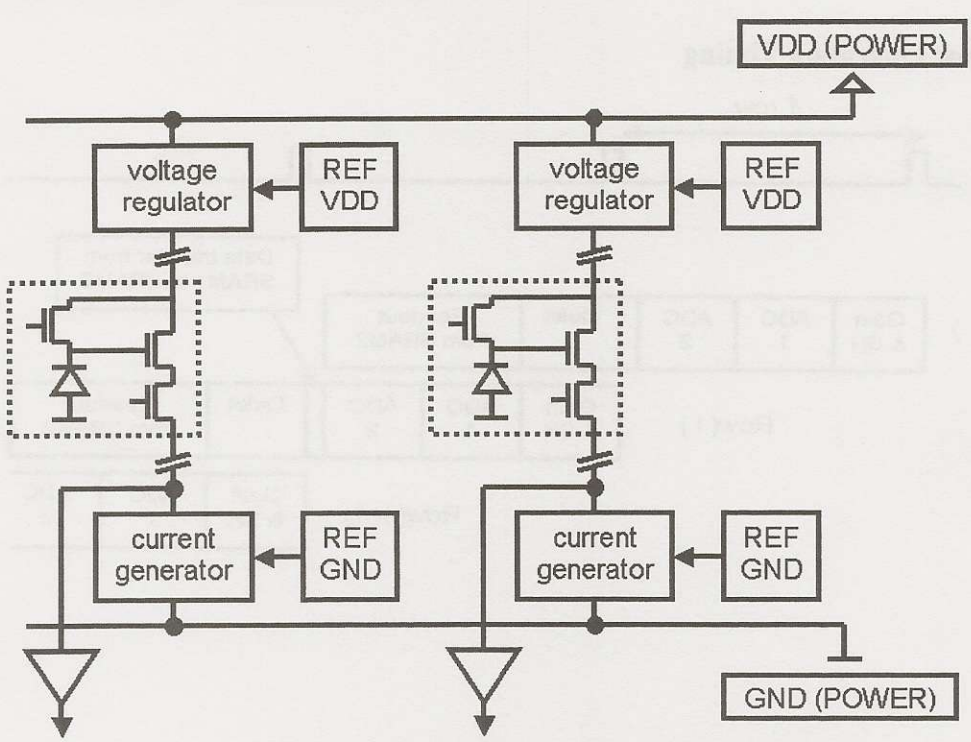

Figure 5 Reproduced Image

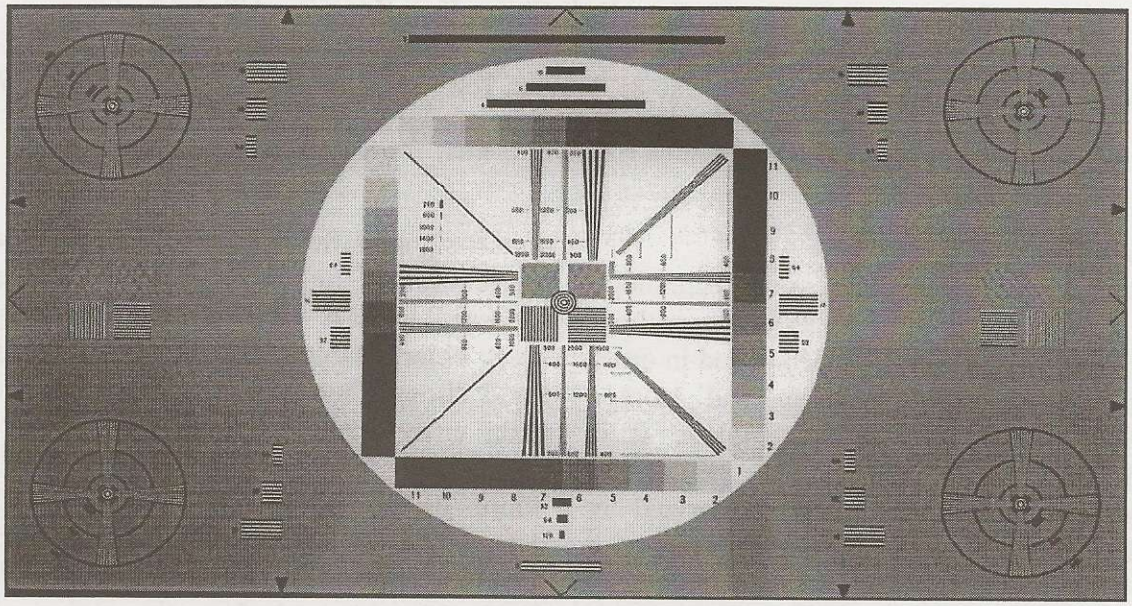

Figure 6 Reproduced Image (Center Portion)