Differential Mode CMOS Active Pixel Sensor (APS) for Optically Programmable Gate Array (OPGA)

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Abstract

A differential mode CMOS active pixel sensor (APS) was designed, fabricated, and tested as part of an optically programmable gate array (OPGA). It was used as a download link between a programmable gate array (PGA) and an optical (holographic) memory, which holds the PGA's configuration data. A differential light encoding scheme was chosen for representing one-bit data to reduce the bit error rate (BER) and the global variation of the programming beams. The number of photons required to change the state of the detector output was measured. The measured thresholds were 800 photons for green (500nm) and 2500 photons for red (650nm) at a 6 μsec integration time. The test chips were designed and fabricated in a 3.3 Volt, 0.35 μm standard CMOS process technology.

I. Introduction

Field programmable gate arrays (FPGA) are widely accepted and have become the industry standard for cost and time efficient prototyping since their introduction in mid-80's. A typical FPGA is composed of configurable logic blocks (CLB) that are used to form logic functions, programmable routing resources, and input/output (I/O) blocks, Fig.1a. Most commonly used FPGA's have a single layer of program memory to hold the chip's configuration data. This configuration data is read in from an external memory regularly or once every system power-up [1],[2]. Data transfer rates between the FPGA and the external program memory can be in the range of 100Mbit/sec which results in configuration times of tens of milliseconds for a medium size FPGA. This clearly manifests a huge overhead compared to the system clock rates of nanoseconds that has prevented users from fully exploring the dynamic characteristics of FPGAs.

There are several different FPGA design approaches proposed to reduce configuration time. One method is to use an addressable SRAM array to store the configuration data, and reconfigure the FPGA partially as in the Xilinx 6200 Series devices, [3]. Another method is to use multiple layers of local memories to hold the full chip configuration data, and switch the layers during configuration. This is known as a multi-context design approach and has been proven to be a very effective solution in terms of reconfiguration time when the context depth is low. However, there exists a trade off between depth of context memory, cost, size and functionality of the multi-context FPGA. With increasing context memory depth, fewer and fewer functional blocks can be integrated in a given size silicon area, [4]. A compromise can be found if the main configuration memory is kept on the physical layer of the FPGA chip and the context memories are transferred onto another medium, such as optical (holographic) memories, [4]. We have called such an FPGA an Optically Programmable Gate Array (OPGA). In this device the computation still runs on the configurable logic blocks and the signals are routed among the blocks through programmable routing blocks as in the conventional FPGA, but the configuration pages are held in holographic memories and brought into the chip optically in parallel. Holographic memories can hold a very large number of context pages on a single hologram without effecting the cost or number of functional blocks of the FPGA, [5]. In terms of full-chip configuration time and depth, this parallelism makes OPGAs much more efficient than context-based FPGAs with only the additional cost of local optical detectors that can be distributed in large or small sized arrays among the programmable blocks, Fig. 1b, 1c.

From the electronics point of view detectors with small, distributed arrays are preferable. This is because they do not require any extra routing area to distribute the detected signals among the programmable blocks, Fig.1b. However, from the optical point of view, centralized optical detector arrays are preferable because the quality of the reconstructed hologram does not need to be uniform over the entire chip, Fig.1c. For small, distributed detector arrays, detector timing and control signals should be routed among blocks, which reduces the total number of available routing wires. In the case of centralized detector arrays, configuration data needs to be distributed among the programmable blocks; this also reduces the routing wires. Furthermore, in the

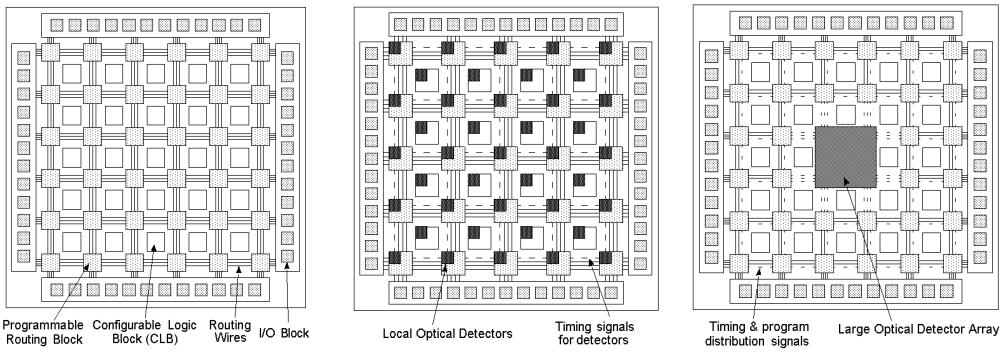

Fig. 1. A generic a) FPGA, b) OPGA with distributed optical detectors, c) OPGA with centralized optical detectors.

centralized case, the program upload parallelism is lost. There exists a trade-off between optical and electronics cost, and complexity. To explore such possibilities, we designed, fabricated, and tested small and large arrays of differential-mode, integration-type CMOS APS photodetectors, and integrated them into a custom designed FPGA, [6].

II. CMOS Photodetector Technologies

With both integrating and non-integrating architectures, the image is generally not taken instantaneously for all pixels and then stored prior to readout. Rather, image gathering and readout are intertwined processes. This defines the concept of exposure time. In a direct access imager, the exposure time for a frame coincides with the time needed to read the frame. In an integrating imager, the exposure time starts with the reset of the first pixel in the frame, and ends with the readout of the last pixel. Based on the readout speed, non-integration type photodetectors are much faster then the integration type sensors. Very fast readout speeds up to 200 Mbit/sec has been achieved in standard CMOS technologies with non-integrating type sensors, [7],[8]. However, integration time photosensors outperform their non-integrating counterparts in terms of sensitivity, repeatability and flexibility when the photon flux is limited.

For photosensors used as an optical interface, one important consideration is the number of photons delivered to the photosensitive area. For holograms reproduced on the image plane, this is more pronounced if the resolution and the number of holograms stored in the holographic material are increased. The photon-budget for our system in green light was around 1000 photons per 1-10 us exposure time.

CMOS integrating photosensors can be divided into two major groups in terms of pixel design: passive pixel sensors (PPS), and active pixel sensors (APS). Passive photodiode pixels with a single access transistor utilize the maximum pixel area for the photo-collection purpose, resulting in the highest fill factor (FF) and quantum efficiency, and smallest pixel sizes, [9]. The main problem with passive pixel sensors is their readout noise and scalability. Active pixel sensors (APS) have more complex pixel structures, [10]. A sensor with an in-pixel buffer or amplifier is referred to as an APS. This buffer actively isolates the photo collection region from the readout bus and circuitry. The CMOS APS trades fill factor for improving overall performance that reduces the quantum efficiency, and the number of generated charges. However, this reduction is more than compensated by reduction in read noise resulting in a net increase in signal-to-noise ratio (SNR) and dynamic range (DR). These are further improved by using microlenses on top of each pixel. We chose a photodiode-type (PD) APS in our design.

One problem that is present when dealing with digital information, as with data stored in holograms, is that the light detected by each sensor needs to be converted into a logic value by comparing it to some threshold. The simplest way to perform such conversion is to use differential encoding, [5],[11]. In this scheme, a pair of holographic pixels represents a single bit of data. A differential detector has to be utilized to convert this pair into a digital output. The detector's input range must be large enough to detect different gray level differences.

III. Differential Mode CMOS PD-APS Design

A very small sensor footprint can be utilized in integration-time sensors. In this mode of operation, speed is traded for area, sensitivity and power consumption. Also it is very convenient to explore parallelism with minimal increase in power or chip area.

A detailed circuit diagram of the detector is shown in the Fig. 2. Each pixel unit cell consists of a photodiode (PD), a source follower input transistor, a row select transistor, and a reset transistor. At the bottom of each column of pixels, there is a source follower load transistor, and a readout branch, (the ASP). This branch consists of a sample capacitor (Cs), and a PMOS source-follower. The amplifier (AMP), double sampling capacitor (Cds), amplifier feedback capacitor (Cpa), and the amplifier reset switch form the delta sampling (DS)

circuit with gain. This readout branch is common to an entire column of pixels while every two ASP branches are connected to a comparator to convert the analog branch signals to digital form, (1-bit ADC).

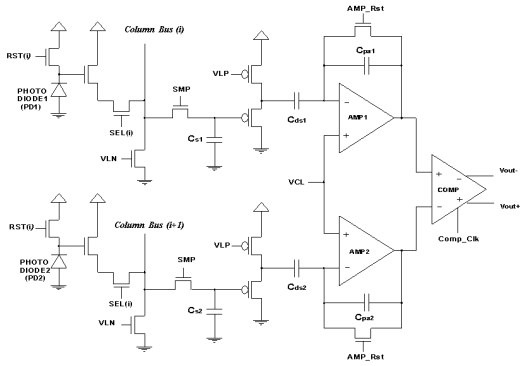

Fig. 2. Differential CMOS PD-APS detector circuit

A differential pair is used as a branch amplifier. Small delta sampling and amplifier feedback capacitances were used. The overall gain of the delta-sampling block is about 20 V/V. The comparator consists of an amplifier and latch combination as shown in Fig. 3, [12]. When the Comp_Clk signal is high, it works as an amplifier with a gain of 10 V/V. Once the Comp_Clk signal goes low, the Mn4 and Mn5 transistors are disconnected from the output nodes, and the amplifier becomes a positive feedback latch. This comparator has reduced kickback noise because the output nodes are isolated from the input.

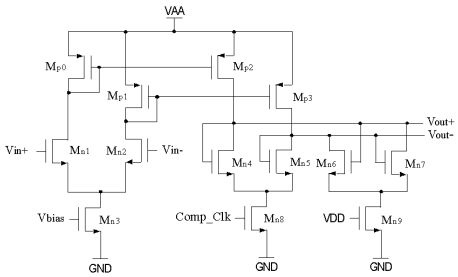

Fig. 3. Amplify-Latch type Comparator.

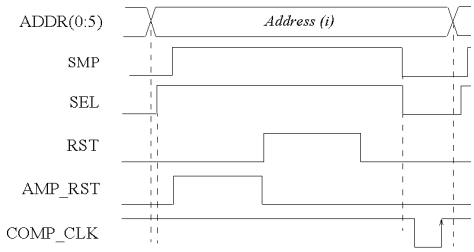

Fig. 4. Timing diagram of the detector

A timing diagram of the readout circuit is shown in Fig. 4. After a row has been selected, both PD1 and PD2 are sampled on to the sampling capacitances, Cs1 and Cs2. Shortly after the row select (SEL) signal goes high, AMP_RST signal is asserted to reset the amplifiers. AMP1 and AMP2 set the voltage at the amplifier side of the double-sampling capacitors, Cds1 and Cds2, to clamp voltage, VCL. The signal sampling phase is finished as soon as the AMP_RST signal is pulled low. The pixel reset level is sampled right after AMP_RST signal is pulled to low by asserting the row reset (RST) signal to high. Assuming that the two readout branches are identical, we can write the voltage difference at the comparator's output node as follow;

$$V_{out} = \frac{C_{ds}}{C_{pa}} \cdot A_{comp} \cdot \alpha \cdot \beta \cdot (V_{pd2sig} - V_{pd1sig})$$

where α is the gain of the pixel source follower, β is the gain of the p-channel source follower, A_{comp} is the comparator gain, $C_{ds}=C_{ds1}=C_{ds2}$ are the double sampling capacitances, $C_{pa}=C_{pa1}=C_{pa2}$.are the amplifier's feedback capacitances, and $V_{sig1,2}$ are the differential pixel voltages. This voltage is used as a seed voltage by the comparator's cross-coupled output transistors when the Comp_Clk signal asserted to logic-0.

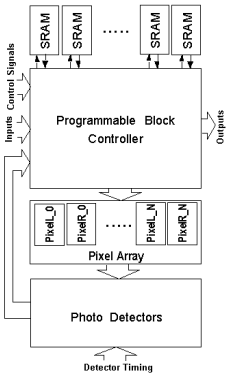

Fig. 5. Generic Optically Configurable Block (OCB)

The Optically Configurable Block (OCB), shown in Fig. 5, is composed of an N-bit local SRAMs to hold the configuration data, a 2N-block of pixels connected to N differential photodetectors, and a programmable block controller. For one clock cycle block configuration, N column parallel detectors need to be used along with 2N pixels. This is the fastest update operation achievable. However, the silicon area required implementing this configuration is the largest. A single differential detector with a 2N-bit pixel array, for example, utilizes minimum area for the optical detector while increasing the OCB update time to N clock cycles. To reduce the OCB area, we choose the single differential detector architecture to implement in our design.

A test chip has been fabricated using 0.35μm CMOS process. The chip contains 12 OCBs in a 5-bit look-up table (LUT) configuration. Each OCB contains a 32-bit block SRAM, a 32x2 array of differential pixels, a differential detector and a 5-bit decoder/driver as a block

controller, as shown in the Fig. 6. A 5µm x 5µm pixel-size was chosen for the design. The area of the 5-bit look-up table OCB is 180µm x 200µm, out of which about the 30% is used by the optical detector circuitry.

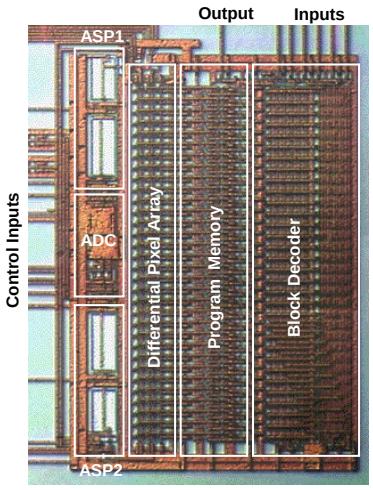

Fig. 6. 5-bit Look-Up Table (LUT) OCB picture

In normal operation, the configuration data stored in the SRAM cells are accessed by the inputs through the decoder. In configuration mode, the data are loaded serially into the SRAM cells. The decoder selects which pair of photodiodes is sensed by the photodetector and in which SRAM cell the detected bit will be loaded.

IV. Photodetector Testing

Testing a differential mode sensor requires a fairly complicated optical setup. To avoid developing such a system, we used an extra metal layer to block partially, or completely, the pixel openings to simulate differential light illumination. This way we would be able to use uniform light during testing.

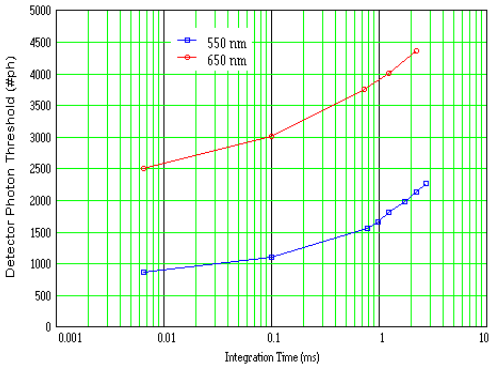

Fig. 7. Photon threshold measurement results

The photon threshold levels of the photodetector were measured for different integration times (6 µsec to 3msec), and light wavelengths (550nm and 650nm). Measured photon thresholds are shown in the Fig. 7. It can be seen from the plot that the shorter the integration time the fewer photons are needed because of the reduced dark current.

V. Conclusion

A differential mode APS was designed, integrated in an optically configurable block (OCB), fabricated, and tested successfully with the photon threshold level of as low as 800 photons at 6µsec integration time.

Acknowledgment

Authors would like to thank Prof. Demetri Psaltis, and his group in Caltech, and Dr. Fai Mok of Holoplex Corporation for their cooperation, and development support.

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