A Micropower Self-Clocked Camera-on-a-Chip

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Abstract

This paper addresses the development of a micropower 176 x 144 CMOS active pixel image sensor that dissipates one-to-two orders of magnitude less power than current state of the art CMOS image sensors. The chip operates from a 1.5 V voltage source and the power consumption measured for the chip running from an internal 25.2 MHz clock yielding 30 frames per second is about 550 μW. This amount enables the sensor to be run from a watch battery. It is believed that this chip is the world's lowest power image sensor and the first image sensor designed for a watch battery operation. The camera-on-a-chip operates as a self-clocked 3-pin sensor (GND, VDD (1.2 - 1.7 V), and DATAOUT). The die occupies 4 mm^2 of silicon.

I. Introduction

Low-power consumption is a fundamental demand for battery-operated devices [1,2] such as cellular phones, portable digital assistants (PDAs), and wireless security systems. Cellular videophones that emerge on the market will utilize state-of-the-art CMOS image sensors consuming 5-30 mW of power. The requirements of the next generation of portable devices to components are expected to be more stringent in terms of power and size.

In traditional CCD based imaging systems, at least one companion chip is required to generate timing, adjust gain, perform analog-to-digital conversion, color processing and image compression. Advanced CMOS technology and submicron design rules yield miniaturized systems-on-a-chip (SoCs) which integrate these multiple functions on the single imaging chip. CMOS systems on a chip also benefit from local signaling which results in smaller interconnect capacitance and, hence, less power. Because the sensor is designed in standard CMOS, application specific functions can be readily embedded into the sensor and prototyping of the designs can occur rapidly at relatively low cost [3].

This paper presents an image sensor which is a prototype of a future generation of micropower image sensors that consume less than 1 mW of power. This value is one-to-two orders of magnitude less than the power in current state of the art CMOS image sensors. The chip is designed for 1.2 - 1.7 V operation, supposedly from one battery, and dissipates 550 μW. The image sensor architecture and analog and digital blocks used in this micropower CMOS active pixel image sensor are described in section II. Summary of a low-voltage sensor design methodology is given in the next section. The final part of the paper deals with the results of the sensor characterization.

II. A Micropower Self-Clocked Camera-on-a-Chip

The sensor's block diagram is shown in Figure 1. The core pixel array consists of 176 (H) x 144 (V) photodiode active pixels [quarter common intermediate format (QCIF)] with a 5 μm pitch. The array of pixels is accessed in a row-wise fashion using a shift register and row driver with a reset bootstrapping circuit so that all pixels in the row are read out into column analog readout circuits in parallel. Each of the 176 column-parallel readout circuits performs both sample-and-hold (S/H) and delta double sampling (DDS) functions, eliminating pixel offset variations and pixel source-follower 1/f noise. The signal is stored in the charge domain. The global charge-sensitive amplifier at the front end of the analog-to-digital converter (ADC) provides a fixed gain for the column charges being read using the column select logic. The amplifier reset and the amplifier signal values are sent to the 8-bit self-calibrating successive approximation ADC. The ADC generates the 8-bit digital output. The digital timing and control logic block generates the proper sequencing of the row address, column address, ADC timing, as well as generates the synchronization pulses for the pixel data going off-chip. The on-chip clock generator generates an internal clock with on-chip bandgap reference circuitry and power-on-reset circuit for the timing and control logic. A signal path from pixel to ADC is shown in Figure 2.

III. Low-Power Design Methodology

Low-power design methodology is considered at all levels – technology, circuit and logic, architecture, algorithm, and system integration. Figure 3 summarizes low-power design steps from process technology to system integration in this research.

For power reduction through circuit/logic design, reduction of the power supply voltage can be a key

element in low-power CMOS image sensors. However, the design of a low voltage CMOS sensor involves several well-known challenges such as a) the reduced dynamic range of pixel, b) the low-voltage MOS switch problem, c) low-voltage opamp and ADC design, and d) low-power internal bias generation. The challenges discussed above are addressed in the following way: a) the pixel voltage dynamic range is increased by using a bootstrapped reset pulse; b) the column analog readout circuit is designed so that only unipolar MOS switches are required. For instance, the S/H switch is of an n-type and is good for sampling pixel signals that are always "low". While the column select switch is of a p-type, which is good at connecting high level signals, such as for the reference voltage, etc.; c) the charge mode readout fixes the readout bus voltage so that the requirements on the amplifier input voltage swing are relaxed. On the other hand, an inverting current-mirror OTA used in this design yields almost rail-to-rail output and a capacitive ADC is selected so as to avoid some low-voltage design problems that would be faced with different types of ADC such as flash, pipelining, or folding converter; d) column readout circuits receive the reference voltage from the readout opamp, eliminating the need for a power consuming reference voltage generator. In this case, the reference voltage is loaded only onto the high impedance opamp input, so the Vref voltage source can be implemented as a high-resistance one.

In addition, the following measures have been undertaken to reduce the sensor power. First, unused blocks such as the pixel current load in the column circuit, and the comparator and opamp in the ADC have been cut from power for the time they do not operate. Second, the column S/H circuit does not have an active buffer. It was replaced with a passive capacitor storage.

IV. Measurement Results

The sensor is implemented in a 0.35 μm, 2 P, 3 M 3.3 V CMOS process with Vtn = 0.65 V and Vtp = -0.85 V. The micrograph of the image sensor is shown in Figure 4. The size of the chip is about 2 mm x 2 mm, which includes the pixel array, row/column logic, analog readout, ADC, biases, on-chip clock generator, timing and control block, and 16 pads. This chip is packaged by 28-pin ceramic leadless chip carrier (CLCC). The chip can operate autonomously with 3 pads (GND, VDD (1.2 - 1.7 V), DATAOUT). Also with an external master clock the chip can operate from 1.2 to 3.6 V power supply. Table I summarizes the sensor chip characteristics at 5 frames per second (fps) and 1.5 V power supply with the external 4.125 MHz clock. The measured power consumption of the overall chip, which includes the pixel array, row/column logic, analog readout, ADC, biases, timing & control block, on-chip clock generator, and pads, is shown in Figure 5 with the internal 25.2 MHz on-chip clock (30 fps) from 1.2 to 1.7 V power supply. At 1.5 V, the measured power consumption is about 550 μW. The estimated overall chip power consumption is 547.5 μW at 1.5 V and 30 fps with the internal 25.2 MHz clock as shown in Table II. Note that the timing and control block consumes about half of total power. Figure 6 shows the measured power consumption of the overall chip at 1.5 V and 2.7V power supply for different frame rates. Images taken with the sensor at 20 and 40 fps with 1.5 V power supply and the external clock are shown in Figure 7. Also images taken with the sensor at 30 fps (25.2 MHz on-chip clock) with 1.5 V and 1.7 V power supply are shown in Figure 7.

V. Conclusion

An active pixel image sensor designed for 1.2 – 1.7 V operation with an on-chip clock generator and 1.2 – 3.6 V operation with an external clock to provide 176 (H) x 144 (V) QCIF 8-bit monochrome video was presented. As a self-clocked sensor, it can be operated with only 3 pads (GND, VDD (1.2 - 1.7 V), DATAOUT). The measured power consumption of the overall chip with the internal 25.2 MHz on-chip clock (30 fps) at a 1.5 V power supply is about 550 μW. Low-voltage image sensor techniques have been successfully tried and the possibility has been shown of wide voltage-range operation (1.2 - 3.6V). This sensor moves us closer to the realization of the 'Dick Tracy' video watch because of its ability to run on a watch battery and its tiny footprint. It is the world's lowest-power CMOS image sensor, and it is expected that the technology will lead to exciting new kinds of wireless digital cameras.

References

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[2] K. B. Cho *et al.*, "A 1.2V Micropower CMOS Active Pixel Image Sensor for Portable Applications", *ISSCC Digest of Tech. Papers*, pp. 114-115, Feb. 2000.

[3] R. A. Panicacci *et al.*, "Active Pixel Sensor Architecture and Design for Multimedia Imaging Applications," *International Workshop on Digital and Computational Video*, Florida, USA, Dec. 1999.

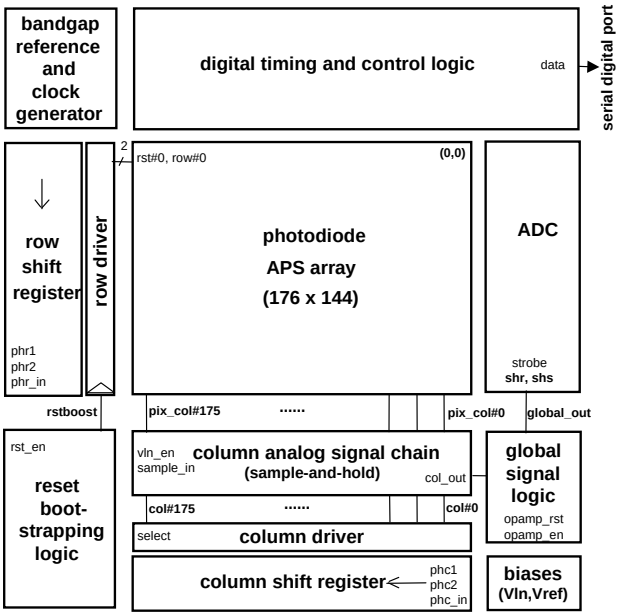

Figure 1: Sensor's block diagram.

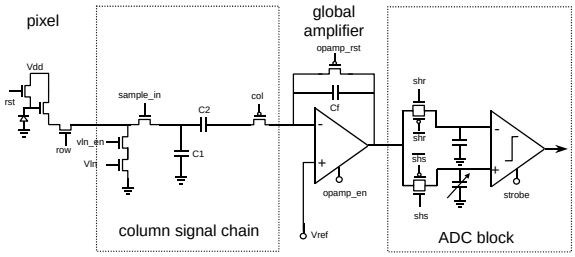

Figure 2: Pixel to ADC signal path.

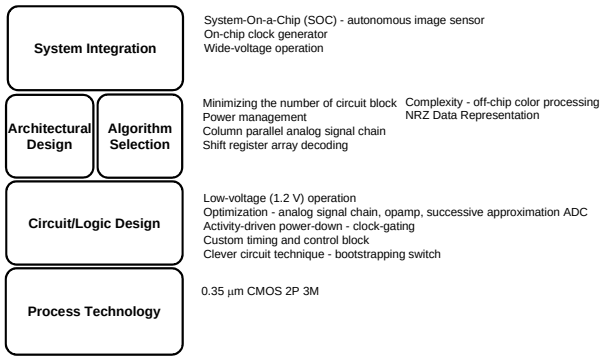

Figure 3: Low-power design steps in this research.

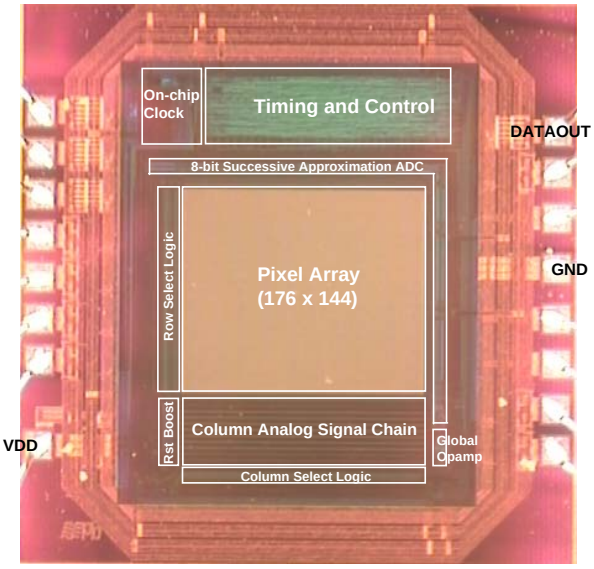

Figure.4: The micrograph of the image sensor.

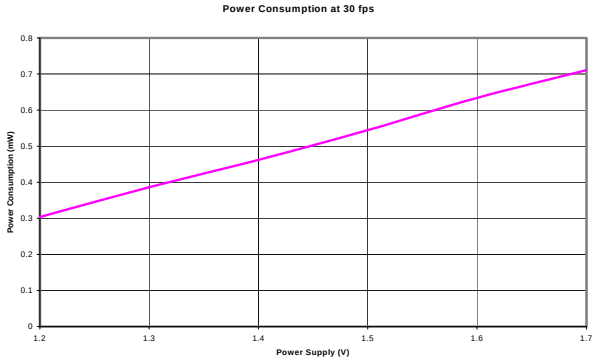

Figure 5: Measured power consumption at 30 fps from 1.2 to 1.7 V with 25.2 MHz on-chip clock.

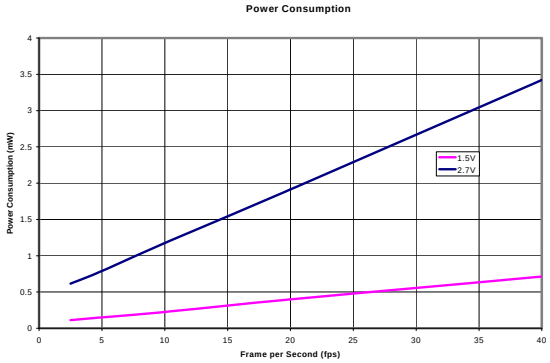

Figure 6: Measured power consumption at 1.5 V and 2.7 V power supply for different frame rates.

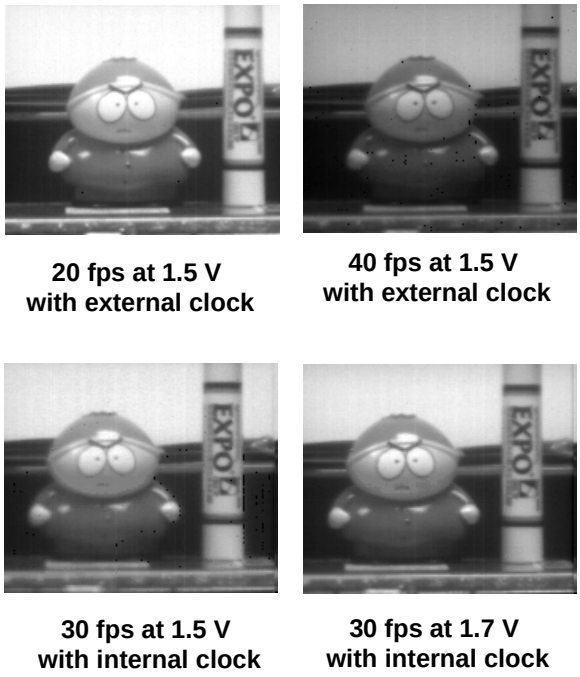

Figure 7: Test images

Table I: Specification and measured sensor performance at 1.5 V and 5 fps.

Technology	0.35 μm, 2 P, 3 M CMOS
Pixel array size	176(H) x 144(V) (QCIF)
Pixel size and type	5 μm x 5 μm Photodiode APS
Pixel fill factor	30 %
Chip size	2 mm x 2 mm
Sensor output	8-bit serial digital
On-chip ADC	8-bit single successive approximation
ADC DNL/INL	1 LSB / 2 LSB
Conversion gain (pixel PD-referred)	34 μV/e-
ADC conversion gain	3.5 mV/LSB
Dark signal	6.97 LSB/sec or 24.4 mV/sec or 718 e-/sec
Saturation (pixel PD-referred)	253.2 LSB or 886.2 mV or 26,065 e-
Noise	0.85 LSB or 3.0 mV or 88 e- r.m.s.
Operating voltage	1.2 – 3.6 V
Maximum frame rate	40 fps
Maximum pixel readout rate	1 Mpix/sec
Power consumption	550 μW at 1.5 V, 30 fps, 16 pads

Table II: Estimated chip power portfolio with 30 fps at 1.5 V power supply.

Main components	Current (μA)	Quantity	Average current (μA)
Column analog signal chain (vln^)	1.4	176 x (1/50)^^	5
Global opamp	30	1 x (1/2)^^	15
ADC (comparator)	16	1 x (1/4)^^	4
Biases (Vln + Vref)	16	1	16
Peripheral (row & col logic + rst bootstrapping circuit + drivers)	20	1	20
Clock generator	75	1	75
Timing and control	170	1	170
Dataout	60	1	60
Total Current (μA)		365	
Total Power (V x I) (μW)		1.5 x 365 = 547.5	
^ peak current : 220 μA ^^ duty cycle factor			