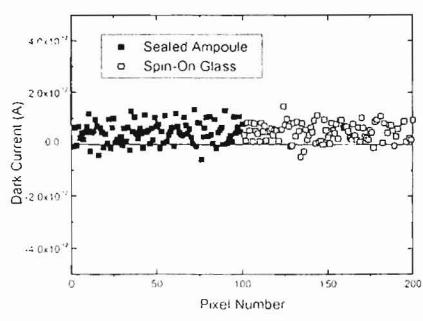


**CWM3** Fig. 2. I-V characteristics of p-i-n diodes formed by the spin-on glass technique as compared with the conventional sealed ampoule technique.

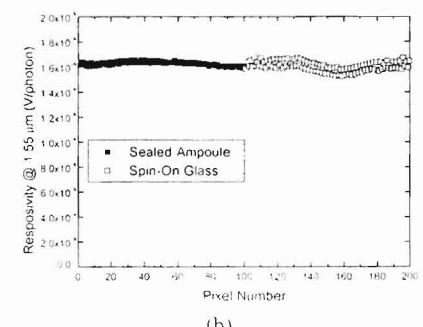
driven into the epitaxial wafer by rapid thermal annealing or furnace heating. Junction quality is equivalent to that achieved with the sealed ampoule technique.

We have fabricated high quality linear photodiode arrays with  $25 \mu\text{m} \times 500 \mu\text{m}$  photodiodes on a  $500 \mu\text{m}$  pitch using both the spin-on glass and sealed ampoule techniques. These have been integrated into self-scanned FPA incorporating CMOS readout integrated circuits (Fig. 1). The CMOS readouts contain a capacitive transimpedance amplifier (CTIA) within each pixel that holds its respective photodiode at zero bias.

Figure 2 shows the I-V characteristics of individual pixels. Under reverse bias, the dark current of the spin-on glass photodiode is approximately an order of magnitude higher than that of the sealed ampoule devices. At zero bias, however, where the FPAs are operated, the shunt resistances are nearly identical;



(a)



(b)

**CWM3** Fig. 3. (a) Pixel-by-pixel dark current of spin-on glass and sealed ampoule arrays at  $T = 250 \text{ K}$ . (b) Pixel-by-pixel responsivity to  $1.55 \mu\text{m}$  light.

$2.9 \text{ G}\Omega$  versus  $1.8 \text{ G}\Omega$ . Figure 3 shows the performance of fully integrated FPAs. The dark current is shown in Figure 3a. This fixed pattern noise is a result of the shunt resistance of each photodiode together with the input offset voltage of its CTIA. The response to  $1.55 \mu\text{m}$  light is shown in Figure 3b. The units,  $\text{A}/\text{photon}$ , are a convolution of the photodiode quantum efficiency (electrons/photon) and the CTIA gain ( $\text{V}/\text{electron}$ ). In both cases, the performance of the spin-on glass and the sealed ampoule arrays are nearly indistinguishable.

#### CWM4 (Invited)

3:30 pm

#### 2 K × 2 K high speed CMOS active pixel sensors for Y2K

E.R. Fossum, A. Krymski, Photobit Corp., 135 N. Los Robles Avenue, 7th Floor, Pasadena, California 91101, USA; E-mail: fossum@photobit.com

We are developing a 4 M pixel CMOS active pixel image sensor for 200 fps (800 M pixel/s) high speed visible imaging applications. This sensor development is based on our previous design and characterization experience with both our  $1280 \times 720$  pixel, 60 fps progressive scan CMOS APS (60 M pixel/s), and our  $1024 \times 1024$  pixel, 500 fps (500 M pixel/s) progressive scan CMOS APS. The former had an on-chip 10 b analog-to-digital converter (ADC), and the latter an on-chip 8 b ADC. The latter is presently the world's highest throughput image sensor, to the best of our knowledge. It dissipates under 400 mW at 500 fps and operates from an approximately 66 MHz master clock with 8 parallel output ports of 8 b each (64 b).

In this talk, first the CMOS APS technology will be generally reviewed. Then the technical issues associated with the development of this sensor will be discussed. This will include issues associated with the pixel (quantum efficiency, crosstalk, etc.), the analog signal processing circuitry, the ADC, and the readout multiplexer. An assessment of trends and projected performance for the next few years will be attempted.

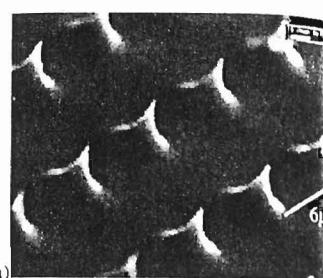
#### CWM5

4:00 pm

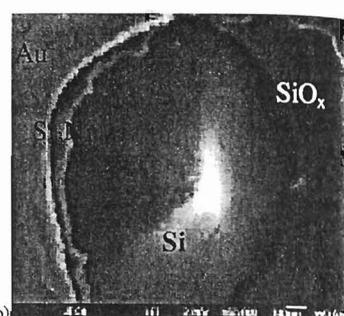
#### Optically excited electron emission from silicon field emitter arrays

K.X. Liu, J. Campbell, J.P. Heritage, Dept. of Electrical and Computer Engineering and Dept. of Applied Science, Univ. of California, Davis 95616, USA; E-mail: kxliu@ece.ucdavis.edu

Very high electric field ( $>0.1 \text{ V}/\text{\AA}$ ) applied across plates of a vacuum capacitor can induce current flow from the cathode to anode even at room temperature. This process, known as field emission, arises when the electron tunneling probability to the vacuum increases as the vacuum barrier width decreases. In 1928, Fowler and Nordheim<sup>1</sup> described a theory of field emission from planar metal surfaces. Interest in field emission as a source for vacuum electronics



(a)



**CWM5** Fig. 1. SEM images of (a) an un gated Si emitters at  $6 \mu\text{m}$  pitch and (b) a gated emitter.

applications has renewed in the last few decades, as microfabrication of metallic semiconductor tips with sub-micron size has become possible. Field emission at the sharp tips and micron scale proximity of a common anode, or gate, at substantial field emission currents at practical potentials ( $\sim 100 \text{ V}$ ). Metallic and semiconductor tips have been studied for potential applications in flat panel displays at cold CW cathodes for microwave vacuum electronics.<sup>2,3</sup>

We have fabricated both electrically (triode) and un gated (diode) arrays of emitters in silicon. Field emission current semiconductors, unlike metals, may be increased by modifying the reservoir of carriers through doping and/or optical injection. Pulsed optical excitation offers the possibility of high peak current and short duration in the vacuum.<sup>4,5</sup> When compared to negative electron affinity photocathodes,<sup>6</sup> field emission devices are much less subject to poisoning and are capable of high quantum yield over longer wavelengths. We report on the measurements of efficient CW photo-induced emission from silicon tip arrays as well as saturation behavior and nanosecond temporal response.

We fabricated field emission arrays of  $1 \mu\text{m}$  thick p-type silicon ( $1-10 \Omega \cdot \text{cm}^2$ ) substrates. The silicon emitters were formed by a dry etching process followed by oxidation and sharpening.<sup>7,8</sup> Measurements reported were obtained on a  $1 \text{ mm} \times 1 \text{ mm}$  (50  $\mu\text{m}$  array having  $20 \mu\text{m}$  pitch. Figure 1(a) shows SEM image of an array of un gated emitters at  $6 \mu\text{m}$  pitch, and Fig. 1(b) shows an SEM image of a single gated silicon emitter with tip radius less than 100 nm. The Au coated gate surrounds the tip.

The dark field emission measurement of anode current (Fig. 2) in a triode configura-