Wide Intrascene Dynamic Range CMOS APS Using Dual Sampling*

Orly Yadid-Pecht, *Jet Propulsion Laboratory, Pasadena, CA USA*
Eric R. Fossum, *Photobit, La Crescenta, CA USA*

Abstract

A CMOS active pixel sensor that achieves wide intrascene dynamic range using dual sampling is reported. A 64x64 element prototype sensor with dual output architecture was fabricated using a 1.2 μm n-well CMOS process with 20.4 μm pitch photodiode-type active pixels. The sensor achieves an intrascene dynamic range of 109 dB without nonlinear companding.

1. Introduction

Scenes imaged with electronic cameras can have a wide range of illumination depending on lighting conditions. Scene illuminations range from 10^{-3} lux for night vision, 10^{2} to 10^{3} lux for indoor lighting, to 10^{5} lux for bright sunlight, to higher levels for direct viewing of other light sources such as oncoming headlights. The intrascene dynamic range capability of a sensor is measured as 20log(S/N), where S is the saturation level and N is the r.m.s. read noise floor measured in electrons or volts. Typical charge-coupled devices (CCDs) and CMOS active pixel sensors (APS) have a dynamic range of 65-75 dB. To permit the use of the sensor in a variety of lighting conditions, both mechanical irises and electronic shuttering techniques are utilized.

Wide variations in intrascene illumination can arise in several situations such as in night driving, observation of landing aircraft, and in space. Increased intrascene dynamic range operation has been demonstrated through the use of companding pixels [1,2,3,4,5]. Drawbacks to this approach include non-linear output that makes subsequent signal processing (e.g. for color) difficult, an increase in fixed pattern noise, and (typically) large temporal noise. Wider dynamic range through judicious resetting of pixels has also been reported but this requires either a priori information about scene brightness [6,7,8], or complicated, large pixels [9]. A new CCD approach that uses two storage sites per interline transfer CCD pixel has been reported where two signals from two independent integration intervals within the frame period are stored [10]. Implementation of this "hyper-D range" CCD architecture requires complicated CCD pixel design with low fill factor and requires twice the charge transfer speed for CCD readout.

In this paper, a new approach to achieving wide intrascene dynamic range is proposed and demonstrated using CMOS APS technology [11].

2. Dual Sampling Approach

In the traditional photodiode-type CMOS APS [12] operating in normal mode, a particular row is selected for readout. The sensor data from the selected row is copied simultaneously for all columns onto a sampling capacitor bank at the bottom of the columns. The pixels in the row are then reset, read a second time, and a new integration is started. The capacitor bank is then scanned sequentially for readout. This scan completes the readout for the selected row. The next row is then selected and the procedure repeated.

The row readout process thus consists of two steps: The "copy" step, which takes time T_{copy}, typically 1 to 10 μsec, and the readout scanning step, which takes time T_{scan}, typically 100 nsec to 10 μsec per pixel. If there are M pixels in a row (i.e. M columns), then the total time for row readout, T_{rro} , is $T_{rro} = T_{copy} + M\,T_{scan}$. The total time to read out a frame with N rows is $T_{frame} = NT_{rro}$. This time is also the integration time for the conventional CMOS APS.

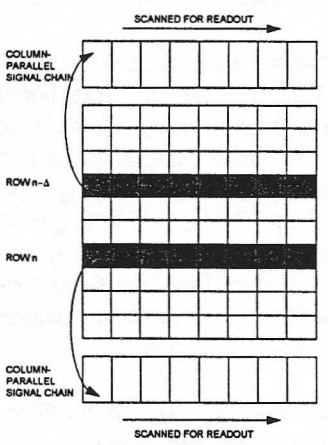

Figure 1. Schematic illustration of dual-sample, dual output imager architecture. Data is fused off-chip.

The architecture of the new wide intrascene dynamic range (WIDyR) approach is shown in Fig. 1. In the new architecture, a second column signal processing chain circuit has been added to the upper part of the sensor. As before, row n is selected for readout and copied into the

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lower capacitor bank. Row n is reset in the process. However, immediately following, row n-Δ is selected and copied into the upper capacitor bank. Row n-Δ is also reset as a consequence of being copied. Both capacitor banks are then scanned for readout. The row readout time has now been increased according to:

$$T'_{rro} = 2T_{copy} + MT_{scan}$$

Since $MT_{scan} >> T_{copy}$ in most cases, $T'_{rro} \simeq T_{rro}$. The total time to readout a frame is also insignificantly affected. However, the integration time for pixels copied into the lower capacitor bank is given by:

$$T1_{int} = (N-\Delta)\, T'_{rro}$$

and the integration time for the pixels read into the upper capacitor bank is

$$T2_{int} = \Delta\, T'_{rro}$$

The output data thus contains two sets of pixel data; one taken with integration time $T1_{int}$, and the second with time $T2_{int}$. For example, when N=512 and Δ=2, then the ratio of $T1_{int}$:$T2_{int}$ is 255:1.

The intrascene dynamic range capability of the sensor is extended by the factor $T1_{int}/T2_{int}$. For example, a sensor with 72 db dynamic range (12 b) when operated in the normal mode is extended by 48 db (8 b) in the above example to 120 dB (20 b). For N=1024 and Δ=1, the dynamic range of the sensor could be extended by 10 bits to a total of 22 bits. The bright portions of the image are viewed best through the short integration time (upper) column parallel signal chain, and darker portions of the image are viewed best through the long integration time (lower) column parallel signal chain. Off-chip fusion of the two images can be performed either linearly (e.g. bit concatenation) or non-linearly (e.g. addition).

The row delay Δ can be set to zero. The short integration period $T2_{int}$ is then the time between the two copy processes. A small delay δT can be inserted to adjust the length of the short integration period so that $T2_{int} = \delta T$. The long integration period $T1_{int}$ is given by:

$$T1_{int} = NT'_{rro} = N\,(2T_{copy} + MT_{scan} + \delta T)$$

In the case where Δ is set to zero, the capacitor banks are loaded with data from the same row and fusion of the short and long integration images can be readily performed on chip if desired.

The dual sampling approach offers several important advantages over the previous approaches described above. First, linearity of the signal is preserved. Second, no modification to the standard CMOS APS pixel is required to achieve high dynamic range so that fill factor and pixel size can be optimized. Third, the low read noise of the CMOS APS pixel is preserved. Fourth, the WIDyR operation can be optionally employed, depending on control signals to the chip, without sacrifice of sensor performance.

Modifications to this approach can also be envisioned. For example, a single capacitor bank could be used, with the data scanned out between copying the long integration period pixel data and the short integration period pixel data. The technique could also be extended to more than two samples per frame resulting in a series of data for each pixel each with a different integration time. The approach can also be used with other types of non-CCD pixels such as passive CMOS pixels or other active pixels.

3. Sensor Design and Operation

The sensor is implemented as previous CMOS APS devices [12] with two modifications. First, a second capacitor sampling bank and column scan decoder has been added to the upper part of the array. Second, a separate row select decoder was added to other side of the array to expedite selection of two different rows. Row decoders on both side have tri-state buffers to eliminate contention issues. In fact, a single row decoder with more complicated row address sequencing could accomplish the same functionality.

The sensor was implemented using the HP 1.2 μm n-well CMOS process available through MOSIS. A photodiode-type active pixel with 20.4 μm pixel pitch and 15% designed fill-factor was used. The same pixel has been used previously with good results [6]. Total chip size was 2.8 mm x 2.8 mm.

4. Experimental Results.

The sensor was initially tested in normal mode. A saturation level of 700 mV and a read noise floor of 160 μV at 100 kpixels/sec was measured, for a normal-mode dynamic range of 72.8 dB (12 b). Conversion gain previously measured for these pixels was ~~3.5~~ μV/e- corresponding to a read noise of 46 e^- r.m.s. Output-referred dark current was measured to be 14.8 mV/sec. Fixed pattern noise was measured to be 20 mV p-p or 2.8% saturation (there was no on-chip FPN suppression circuitry). These results are consistent with previous photodiode-type CMOS APS devices.

The sensor was operated in WIDyR mode using the dual outputs. An example of the output is shown in Fig. 2 for the short integration period (left) and long integration period (right), where the two outputs are 4 rows apart improving the intrascene dynamic range by 15:1 or 3.75 bits. Additional data is shown in Fig. 3 where sensor output signal is plotted as a function of sensor integration time for various row delays (Δ). Good linearity is demonstrated. With a minimum experimental row delay of Δ=1 row, the intrascene dynamic range is extended by approximately 64 times to 109 dB (18 b). Total sensor power when operating at 100 kpixels/sec per output channel with a 5V supply was measured to be 19.5 mW.

5. Conclusions

A CMOS APS with wide intrascene dynamic range using dual sampling and dual outputs has been demonstrated. Extension of dynamic range from 72 dB in normal mode to 108 dB in the WIDyR mode was shown. The approach offers the opportunity to capture images with intrascene dynamic range limited not by the detector, but by optical effects such as stray light and internal reflection.

Figure 2. Experimental sensor outputs with dual sampling with 4 row delay yielding exposure ratio of 15:1 for 2 different levels of faceplate illumination. Left images are output of short integration channel, and right images are output of long integration channel. Upper pair has lower faceplate illumination than lower pair. Note vertical shift between left and right images corresponding to 4 row delay.

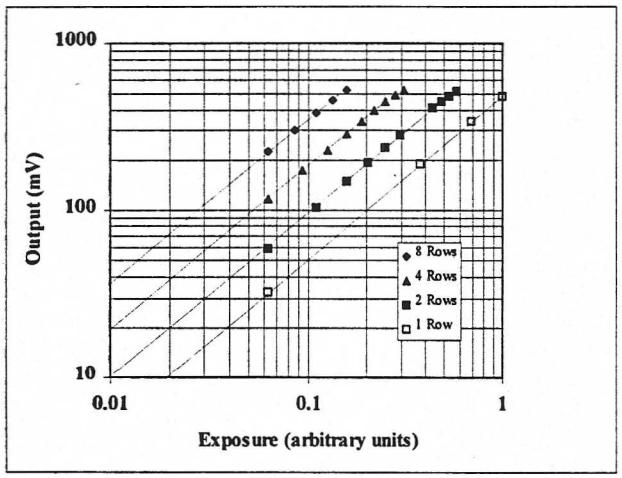

Figure 3. Sensor output as a function of integration time for various row delays.

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7. References

1. Chamberlain S.G. and Lee J.P., "Silicon imaging arrays with new photoelements", wide dynamic range and free from blooming", Proc.1984 Custom Integrated Circuits Conf., Rochester, NY, USA, pp. 81-85, (1984).
2. C. Mead, "A sensitive electronic photoreceptor," 1985 Chapel Hill Conference on VLSI, pp. 463-471 (1985).
3. N. Ricquier and B. Dierickx, "Pixel structure with logarithmic response for intelligent and flexible imager architectures," Microelectronic Engineering, vol. 19, pp. 631-634 (1992).
4. Kub F.J. and Anderson G. W. , "Compressing photodetectors for long optical pulses using a lateral blooming drain structure", IEEE Trans. Electron Devices, vol. ED-40(1), pp. 1740-1744, (1993).
5. Decker S. and Sodini C. G., " Comparison of CCD and CMOS pixels for a wide dynamic range area imager", 1995 IEEE Workshop on CCD's and Advanced Image Sensors, Dana Point, California, USA, April 20-22, (1995).
6. S. Chen and R. Ginosar, "Adaptive sensitivity CCD image sensor," Charge-Coupled Devices and Solid-State Optical Sensors V, Proc. SPIE, vol. 2415, pp. 303-309 (1995).
7. O. Yadid-Pecht, B. Pain, C. Staller, C. Clark, and E.R. Fossum, "CMOS active pixel sensor star tracker with regional electronic shutter," IEEE J. Solid-State Circuits, vol. 32(2), pp. 285-288 (1997).
8. H. Shimamoto, K. Mitani and Y. Fujita, "A dynamic range expansion method for a CMD imager," Solid-State Sensor Arrays: Development and Applications, Proc. SPIE, vol. 3019, pp. 249-255 (1997).
9. Yadid-Pecht O., "The automatic wide dynamic range sensor (AWDRS)", 1993 SID Intl. Symp., Seattle, Washington, pp. 495-498, (1993).
10. Komobuchi H., Fukumoto A., Yamada T., Matsuda Y. and Kuroda T., "1/4 Inch NTSC format hyper-D range IL-CCD," 1995 IEEE Workshop on CCD's and Advanced Image Sensors, Dana Point, California, USA, April 20-22, (1995).
11. O. Yadid-Pecht and E.R. Fossum, "Readout schemes to increase dynamic range of image sensors," NASA Tech. Briefs, vol. 21(1), pp. 32-33 (1997).
12. S.K. Mendis, S.E. Kemeny, R.C. Gee, B. Pain, Q. Kim, and E.R. Fossum, "CMOS active pixel image sensors for highly integrated imaging systems," IEEE J. Solid-State Circuits, vol. 32(2), pp. 187-197 (1997).