Megapixel CMOS APS with Analog and Digital Readout

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Introduction

This paper reports the operation and performance of two 1024x1024-element CMOS active pixel image sensors (APS) with on-chip analog-to-digital conversion (ADC), analog and digital readout signal chain electronics. Previously, a 256x256-element CMOS APS with on chip timing and control was demonstrated by JPL with excellent image quality. The work reported in this presentation is to investigate feasibility of large format APS, the effect of design rule scaling on APS performance, and the demonstration of digital APS readout with on-chip column-parallel single slope ADC.

The two APS imagers reported here include both photodiode-type and photogate-type pixels, with in-pixel source followers, row selection and reset transistors. The chips have been implemented in a 0.55 μm n-well process, have a 11.0 μm pixel pitch, and operate from a +3.3 V supply. They are intended for slow-scan space science applications requiring 100 kpix./sec to 5 Mpix./sec data rate.

Chip Design

The two chips have identical design of readout circuit and control logic. Each sensor has two separate readout signal chains one analog and the other digital. The schematic design of the chip's signal chain (for the photogate approach) is shown in Figure 1. The analog readout signal chain is similar to that reported for the 256x256 CMOS APS "camera-on-a-chip" [1]. It performs correlated double sampling (CDS) to suppress pixel fixed pattern noise, and double delta sampling (DDS) to suppress column dependent fixed pattern noise.

The digital readout signal chain consists of a 1024 column parallel 10-bit single slope ADCs with built-in CDS. A block diagram of the chip architecture is shown in Figure 2. The ramp reference voltage is supplied by a single on-chip ramp generator. This ramp generator takes din0 to din9 (shown in Figure 2) as input to generate the corresponding reference voltages. A block diagram of the chip architecture is shown in Figure 3. The 10 bits decoders are controlled by input clocks to supply the row address and column address for analog or digital mode operation of the chip. The analog outputs are VS_OUT (signal) and VR_OUT (reset), and the digital outputs are D_out0 to D_out9. The analog and digital readout chains are separated by the pixel array. Each imager can be operated in analog or digital readout mode. Layout of the 1Kx1K CMOS APS with on-chip ADC is shown in Figure 4.

Testing Results

Testing results measured through the analog signal chain are summarized in Table 1. Figure 5 shows a full 1Kx1K image from the photodiode based sensor operated in analog mode. The integration time of the image is approximately 2.5 sec which is limited by the speed of the data acquisition board in the computer. NTSC operation has been demonstrated within a window subsection of the chip. Measurement through the digital signal output chain of the image sensors will also be presented. The analog readout circuit and the 10-bit single slope ADC of the imager will be explained in more detail.

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The number of defective pixels including "hot" (high leakage) pixels and missing row & columns constitute less than 5% of the imager pixels. Considering that the chips were fabricated in an experimental 0.55 μm CMOS process, this is an impressive result. Further, the chips with photogate-based APS seems to have an excessive leakage current from the MOSFETs. The presence of a substantial MOSFET leakage has resulted in increase in both the imager dark current, and power consumption from the digital components due to an increase in the off-state current. Experimental data indicates that both analog and digital power dissipation increased with increasing pixel rate. The increase in analog power dissipation does not correspond to the results previously published for the 256x256 format imager [1], and is probably due to an increase in the transient current required to settle signals over larger column capacitive loads.

Conclusions

1Kx1K CMOS APS using 0.55 μm process was designed by JPL and fabricated by National Semiconductor Inc. and the tested and characterized at JPL. Testing results show that the large format APS with smallfeature size (10 micron pixel pitch) is capable of excellent imaging performance. The scaling down of CMOS design rules and pixel size does not appear to introduce any anomaly to the imaging performance of CMOS APS.

Acknowledgment

The research described in this paper was performed by the Center for Space Microelectronics Technology, Jet Propulsion laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration, Office of Space Science.

[1] R. Nixon, S. Kemeny, B. Pain, C. Staller, and E. Fossum, "256x256 CMOS active pixel sensor camera-on-a-chip," *IEEE Journal of Solid State Circuits*, vol. 31, no. 12, pp. 2046-2050, Dec. 1996.

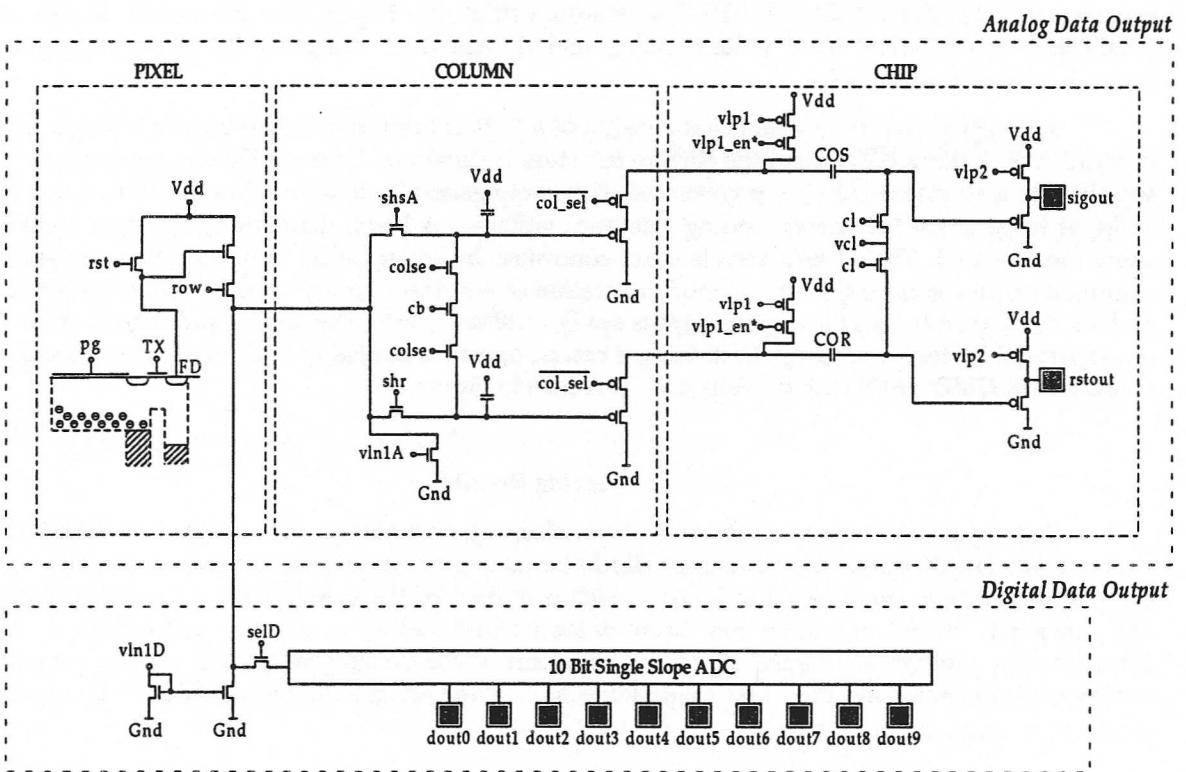

Figure 1. Signal chain of the 1Kx1K CMOS APS chip design.

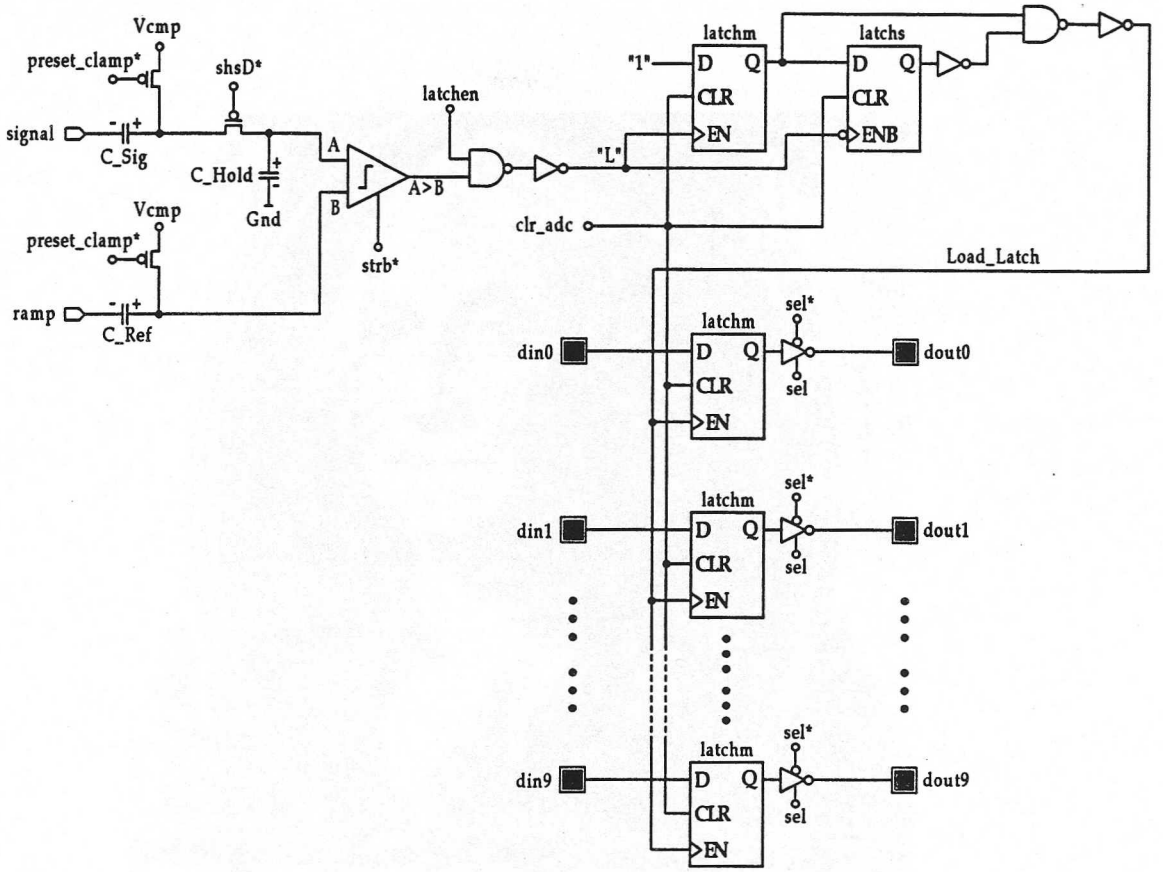

Figure 2. *Schematic of the single slope ADC.*

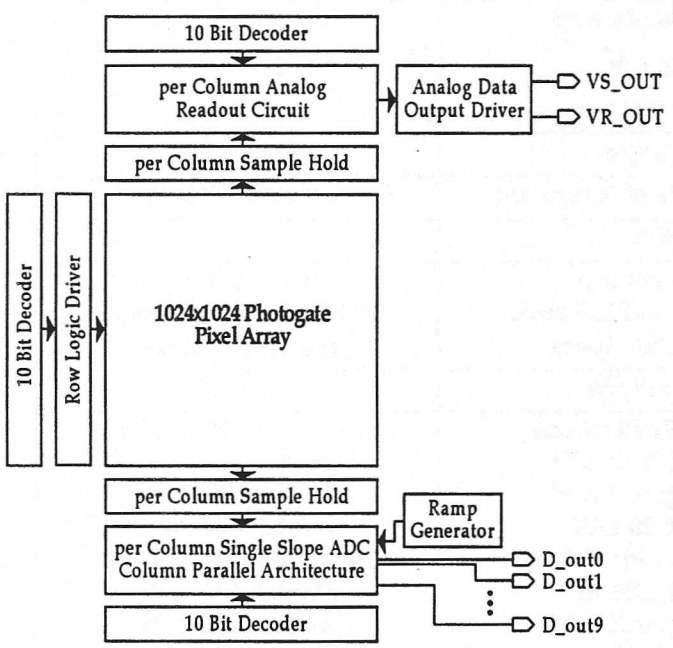

Figure 3. *Block diagram of 1Kx1K CMOS APS chip.*

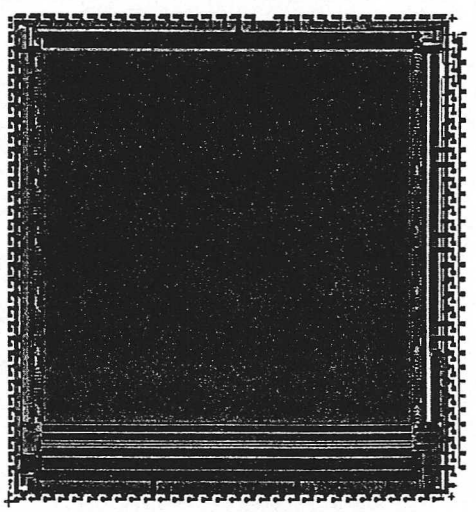

Figure 4. *Layout of 1Kx1K CMOS APS with on-chip ADC.*

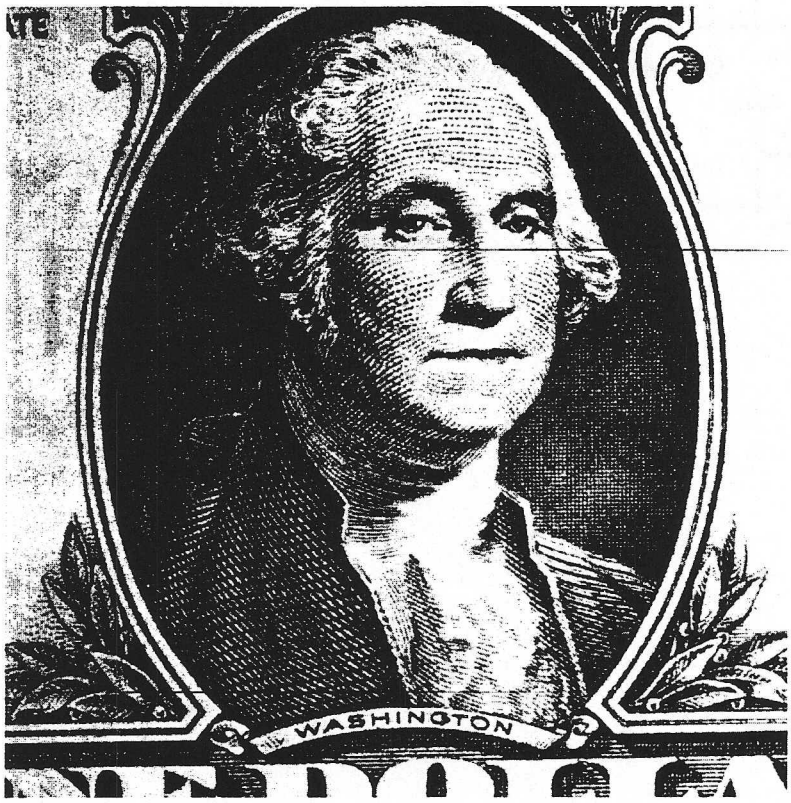

Figure 5. Full Image of 1Kx1K Photodiode CMOS APS from the Analog Output.

Table 1. Summary of testing results measured through the analog signal chain.

Parameters	Photodiode APS	Photogate APS
Saturation Level	655 mV (307,000 e-)	570 mV (41,000 e-)
Conversion Gain	2.1 μV/e-	13.9 μV/e-
Linearity	99.9% @ 90% of Saturation	99.6% @ 90% of Saturation
Peak QE	45%	18%
Fixed Pattern Noise	0.6% Sat p-p (@ 22.3 °C and 159 msec integration time)	0.6 % Sat p-p (@ 22.5 °C and 39.2 msec integration time)
Dark Current	14.9 mV/Sec	371 mV/Sec
Power Consumption	**@ 833 kHz Pixel rate** Digital: 5.77 mW Analog: 14.2 mW Total: 20 mW **@83.3 kHz Pixel Rate** Digital: 2.31 mW Analog: 6.86 mW Total: 9.17 mW	**@ 833 kHz Pixel rate** Digital: 52.8 mW Analog: 22.3 mW Total: 75 mW **@83.3 kHz Pixel Rate** Digital: 48.7 mW Analog: 18.2 mW Total: 66.8 mW