Design of an Image Sensor with On-Chip Oversampling Analog-to-Digital Conversion

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Abstract This paper presents a design of a current-mode active pixel image sensor with on-chip analog-to-digital conversion(ADC). Design and experimental results of a fixed pattern noise(FPN) suppression circuit and a current-mode second-order incremental Δ-Σ oversampling A/D converter are described. Based on the experimental results, design of a current-mode active pixel image sensor with on-chip ADC is reported.

I. INTRODUCTION

An on-focal-plane analog-to-digital conversion(ADC) is highly desirable to improve imaging system performance and reliability and to reduce system size, weight and cost. The approach matches industry trend where A/D conversion is performed as early as possible in a signal chain to avoid analog signal processing and instead utilize digital signal processing, enjoying the benefits of rapidly improving CMOS device technology.

Quantization noise in analog-to-digital conversion can be considered to be white noise distributed from DC to the Nyquist frequency. Thus, it is possible to decrease the quantization noise spectrum by increasing the sampling frequency, since the total noise power is constant. In addition, there are techniques of noise shaping, where most of the quantization noise power is placed outside the signal band and can be removed by low pass filtering, thus yielding higher signal-to-noise ratio. Among the techniques, the Δ-Σ modulation is the most popular scheme. In general, the oversampling converters can be implemented with simple and relatively low precision analog components, while the conventional Nyquist rate converters require high precision analog circuits. The expense is that fast and complex digital signal processing stages are needed. However, its robustness and the use of fine line width digital CMOS devices are matched with the steadily improving CMOS device technology.

Multiple sampling or oversampling of the detector signal can be much more effectively performed on the focal-plane compared to off-chip. Detector's noise level can be resolved with an on-chip oversampling converter without pre-amplification by simply increasing the oversampling ratio.

An on-focal-plane columnwise current-mode Δ-Σ ADC for current-mode active pixel sensors was investigated for high resolution applications. Compared to the conventional voltage-mode approach which is usually a switched capacitor approach, the current-mode approach is expected to be faster and less sensitive to component variations. The critical elements in switched capacitor approach include linear capacitors and the MOS op-amp which is the slowest analog component and the one most vital to conversion accuracy. The current-mode approach uses no MOS op-amp or linear capacitors. The main building block is a current copier cell. In order to realize a practical on-chip columnwise ADC, small area and low power dissipation are required.

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A first-order Δ-Σ A/D converter requires 2^n cycles to perform an n-bit ADC. A higher order Δ-Σ, built by incorporating additional error integrator loops, can speed up the conversion. In this work, a cascade of two first-order stages resulting in an incremental Δ-Σ ADC topology was investigated. Since it consists only of cascaded first-order stages, it is immune to loop instabilities. The rationale for choosing a second-order scheme was to avoid large area and power penalties associated with higher order designs, while allowing vastly improved conversion speeds compared to a first order topology.

II. EXPERIMENTAL RESULTS

a. FPN Suppression

The FPN suppression circuit, shown in Fig. 1, removes the offset current variations between pixels by using a combination of an n-type and a p-type current copier cell. During the ϕ_1 phase, $I_1=I_{off}$ is memorized on the first n-channel current copier cell. During the ϕ_2 phase, $I_2=I_{off}-I_{sig}$ is flowing into the circuit, with the first n-channel copier being in the output phase and the second p-channel copier being in the memorizing phase. During the ϕ_3 phase, with ϕ_4 on and the p-copier being the output phase, this circuit outputs I_{sig}. It exhibits linear transfer characteristics in the input range from 0 to 30μA.

b. Current-Mode Second-Order Incremental Oversampling A/D Converter

Fig. 2 shows the architecture of the second-order incremental Δ-Σ A/D converter. The A/D converter is composed of a Δ-Σ modulator and a decimation filter. One integration cycle consists of four clock phases. The roles of each clock cycle are; 1) memorizing current, 2) copying current, 3) comparing the output current of the integrator, I, with the reference current I_{ref}. The clock phase which perform the particular role in the second loop is shifted by one clock phase, compared to that of the first loop. Table I shows the relationship between the integration cycle and resolution. The modulator was built using 2μm single poly, double metal, twin well CMOS process. An FPGA was used to build the decimation filter. The experimental results for a 12bit operation are summarized in Table II

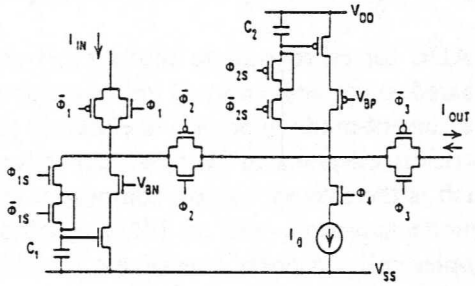

Fig. 1 FPN suppression circuit

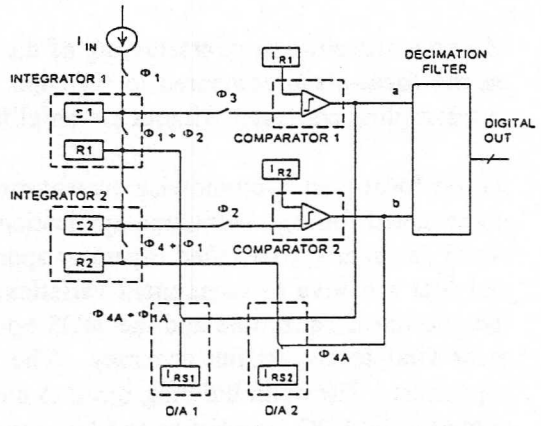

Fig. 2 Architecture of the second-order incremental Δ-Σ A/D converter

Table I. Relationship between ADC resolution and integration cycles p

resolution n (bits)	p
6	12
7	17
8	24
9	33
10	46
11	65
12	92
13	129
14	182

Table II. Experimental Results

Supply voltage	V_{DD}=5V V_{SS}=0V
Power dissipation of the modulator	0.8mW quiescent 1.2mW max.
Resolution	12bits
Reference current	18.5μA
I_{LSB}	4.5nA
Conversion time	177μs
Differential nonlinearity	±1.5 LSBs
Integral nonlinearity	±10 LSBs
Process technology	2μm single poly double metal twin well CMOS
Active area of the modulator	0.15mm^2

III. DESIGN OF AN IMAGE SENSOR WITH ON-CHIP ADC

We consider an image sensor with the on-chip FPN suppression circuits and current-mode second-order incremental Δ-Σ analog-to-digital converters. Fig. 3 shows a block diagram of the image sensor. Each FPN suppression circuit is assigned for each column and its output is fed to an A/D converter. An A/D converter may be connected to each FPN suppression circuit or may be assigned for several FPN suppression circuits with multiplexing.

The sequence of the image sensor operation is shown in Fig. 4. During the horizontal blanking period, the FPN suppression is performed. Next, two reference current sources (I_{R1} and I_{R2} in Fig. 2) and two reference current sinks (I_{RS1} and I_{RS2}) in each modulator are refreshed prior to each A/D conversion cycle. This current set-up operation is performed during the same period of digital data readout. A block diagram of the circuits around the current sources/sinks is shown in Fig. 5. Each current source/sink is composed of a cascoded current copier cell of which relative accuracy is quite good. Fig. 6 shows a pulse timing diagram for the reference current set-up. Then, A/D conversion follows.

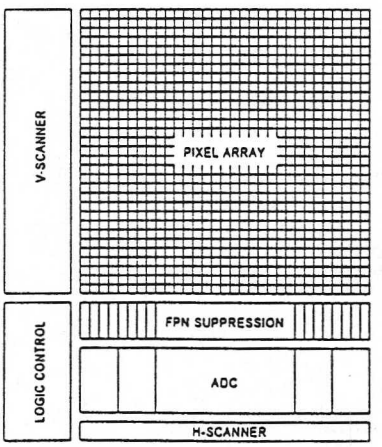

Fig. 3 Block diagram of the image sensor

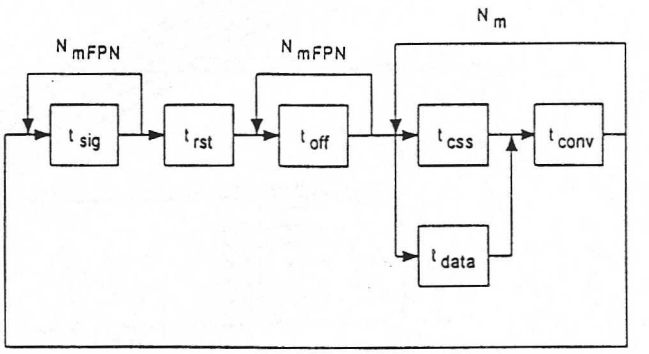

Fig. 4 Sequence of the image sensor operation

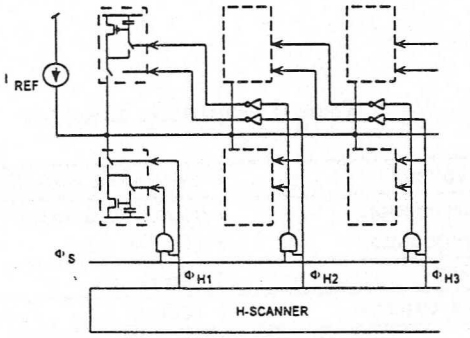

Fig. 5 Block diagram of the current set-up circuits

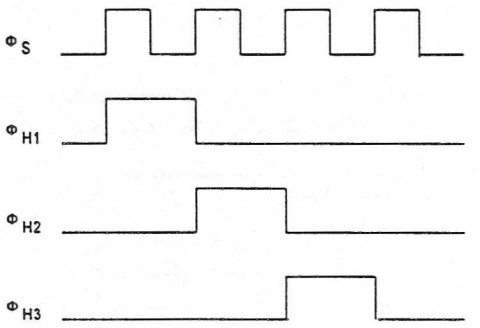

Fig. 6 Pulse timing for the reference current set-up

The A/D converter including a decimation filter which consists of static CMOS logic gates in a 2 μm design rule occupies approximately 80 × 5,000 μm^2 ($0.4mm^2$). In order to realize a practical image sensor, the silicon area of the FPN suppression circuits and the A/D converter as well as scanning circuits should be decreased with scaled CMOS devices. Power supply voltage is also reduced to 3.3V for CMOS devices of which feature size is below 0.5 μm.

The operation of the circuits with 0.5μm CMOS and 3.3V supply has been confirmed by SPICE simulation. The transistor counts of the decimation filter can be reduced using a dynamic domino logic. It is estimated from the current layout that the ADC will occupy about 40 × 2700 μm^2 (0.11 mm^2) silicon area with standard 0.5 μm design, while maintaining the same capacitance value in the analog part. Thus, one ADC can be assigned for every 4 columns, supposing the pixel(column) pitch is 10μm. Fig. 7 shows the estimated relationship between the frame rates and the number of rows. Assumption include; N × N pixels, 0.5μm design rule, the pixel reset time of 2 μs. The figure shows the frame rates in case where one ADC is assigned for every 4 columns for 1024 ×1024 pixels, 4 columns for 512 × 512 pixels, 2 columns for 256 × 256 pixels, and 1 column for 128 × 128 pixels, respectively. The pixel size varies accordingly. The frame rate of a 1k × 1k image sensor with 10μm pixel size is estimated to be 1fps for 12 bit operation (p=92). For a 128 × 128 image sensor with 40μm pixel pitch, the frame rate of 25fps is possible for 13 bit operation (p=129). For a 1k × 1k image sensor, chip size and power dissipation are expected to be 12 × 15 mm^2 and 115 mW, respectively.

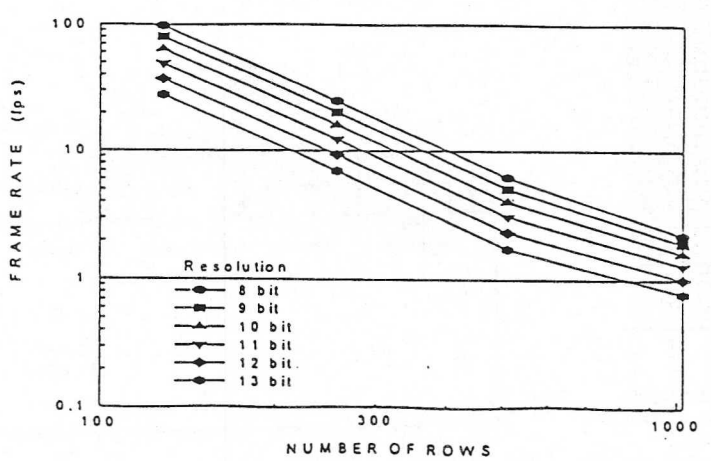

Fig. 7 Estimated relationship between frame rates and the number of rows.