

# A Single Chip CMOS APS Digital Camera

Brita H. Olson, Tim Shaw, Bedabrata Pain,  
Roger A. Paniccaci\*, Barmak Mansoorian\*, Robert H. Nixon\*, and Eric R. Fossum\*

Jet Propulsion Laboratory  
California Institute of Technology  
mail stop: 300-315  
Pasadena, CA 91109

\* Photobit  
2529 Foothill Blvd.  
La Crescenta, CA 91214

e-mail: brita.olson@jpl.nasa.gov

## Abstract

There is an enormous demand for low power, highly integrated image sensor systems. CMOS based Active Pixel Sensor (APS) technology enables this progression. We demonstrate a very low power, highly integrated, programmable, complete digital camera-on-a-chip based on CMOS APS technology. It features on-chip analog-to-digital converters (ADCs) in addition to full timing and control. All analog references required for proper imaging and digitization are generated on-chip with programmable digital to analog converters (DACs). Thus the camera has a complete digital interface. It can be programmed to support a variety of imaging operations and interface configurations through a single digital input pin, facilitating integration with external systems. The integration of this circuitry on the sensor does not degrade 8-bit imaging at normal operating speeds. A variety of power reduction features make it an ideal candidate for power constrained, portable, miniaturized applications. It is currently scheduled to be included in a highly miniaturized ( $< 2 \text{ inch}^2$ ) battery operated digital camera with a wireless interface.

The imager, shown in Figure 1, is a  $256 \times 256$  photogate<sup>1</sup> array with  $20.4 \mu\text{m}$  pixel pitch and a 21% fill factor. It includes 256 column parallel 10-bit successive approximation ADCs with internal correlated double sampling (CDS) and offset correction. All internal analog references are generated by four on-chip digitally programmable 5-bit DACs. Circuitry in the DACs, pixel source followers and ADCs is disabled when not in use for power reduction. The imager has been fabricated in a  $1.2 \mu\text{m}$  N-WELL HP process through Mosis and is  $9.3\text{mm} \times 11.2\text{mm}$ . At its current format the ADCs, the imager and the control circuitry each require about a third of the total area (see Table 1). The design is scaleable to larger array sizes with existing  $.7 \mu\text{m}$  design rules; at a  $1\text{K} \times 1\text{K}$  format, the imager would occupy roughly 80% of the total area.

The camera is programmed and receives commands through a single digital pin; therefore no command buffering is required. It has a fully programmable exposure time, implemented as a rolling shutter, which can be greater than or equal to the frame read time. It also has fully programmable windowing and subsampling. These options when enabled allow for accelerated image output.

Additionally the camera can be programmed to support a number of imaging modes as well as digital input and output interfaces. Although primarily a digital still camera, it can be configured to take images continuously. After acquiring a digital still image, it automatically enters a low power ( $40 \mu\text{W}$ ) idle mode, implemented by turning off analog circuitry. It also has a fully programmable warm-up timer that can be used to delay image capture.

To ease integration requirements, the camera can be programmed to accommodate a number of interfaces. For example, it can produce serial or parallel output with a variety of data formats; it can support full or half duplex protocols, generate vertical and horizontal frame syncs, perform serial input clock recovery and can handle various system data rates. Only 5 wires

the imager. To minimize post packing footprint area, the 8 pins are located on one side of the imager. Non-essential digital pins are set to a known state when floating so they do not disrupt chip operation.

The signal chain and examples of timing diagrams are shown in Figure 2. The pixel control signals are similar to those used in other APS photogate imagers and are described in more detail in reference 1; a difference in this implementation is that the floating diffusion is usually reset, thus soft reset is not required. In operation, the reset and signal pixel values are first sampled; following this they are subtracted, digitized and output. With serial output, the row readout time is dominated by the time required to readout the data, as shown in Figure 2 c. With parallel output, roughly 50% of the row readout time is required to output the data.

The camera can be programmed to accommodate a variety of input and output data rates as well as clock rates. For example, one can have separate input command and output data rates. This flexibility is achieved by using separate programmable clocks, derived from the input clock, to control various on-chip operations. Two of the clocks affect the sample and hold time and the ADC conversion rate. In this way, the sample and hold time and the ADC conversion time can be controlled separately and be independent of the input clock rate. Thus, the settling time for these two operations can be held constant for a number of input clock rates

The camera has been designed to support up to a 60 Hz frame rate with parallel output and up to a 14 Hz frame rate with serial output. Using serial output, the chip requires 1.7 mWatts for the digital control circuitry and 9.2 mWatts for the analog circuitry for a total of 10.9 mWatts at an output rate of 85 kpixels/sec. Of the 9.2 mWatts of analog power, 4.6 mWatts are used for two voltage supplying DACs; 2.4 mWatts are used for two current supplying DACs and the remaining 2.2 mWatts for the pixel amplifiers and the ADCs. When the camera is only integrating, the chip power drops to 6.5 mWatts, using 1.7 mWatts and 4.8 mWatts for digital and analog circuitry, respectively; at this time the pixel amplifiers, the ADCs, and the two current DACs are off and the voltage DACs are on, but not switching.

**Acknowledgments:**

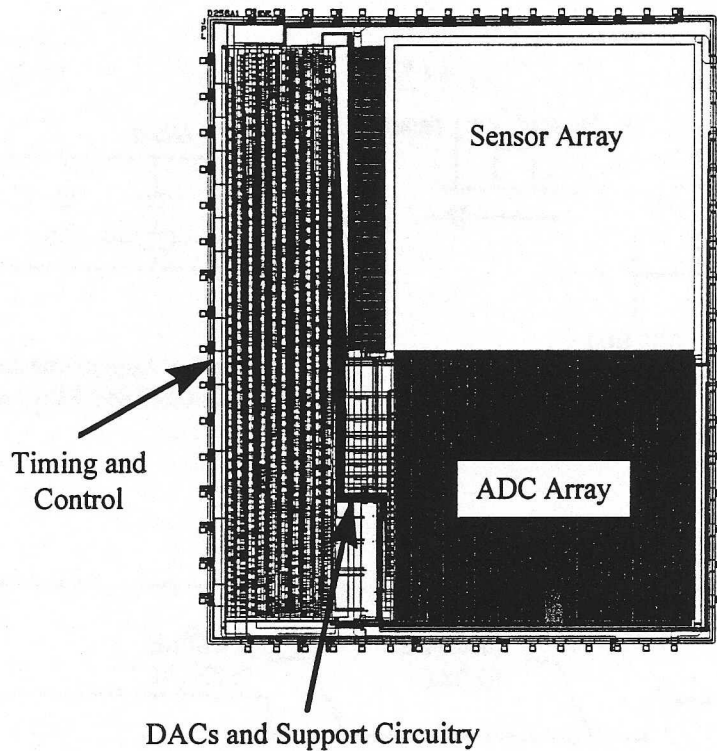
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**References:**

1. S. M. Mendis, S. E. Kemeny, R. C. Gee, B. Pain, C. O. Staller, Q. Kim, E.R. Fossum, "CMOS Active Pixel Image Sensors for Highly Integrated Imaging Systems," IEEE J. Solid State Circuits, Vol. 32 No. 2, pp. 187-97, 1997.

|                    | current 256 x 256<br>area , (percentage of chip area) | 1024 x 1024 .5 $\mu$ m HP<br>area , (percentage of chip area) |
|--------------------|---|---|
| Sensor Array       | 27 mm <sup>2</sup> (37%)                              | 150 mm <sup>2</sup> (79%)                                     |
| ADC bank           | 24 mm <sup>2</sup> (33%)                              | 33 mm <sup>2</sup> (17%)                                      |
| DACs               | .5 mm <sup>2</sup> (<1%)                              | .2 mm <sup>2</sup> (<1%)                                      |
| Timing and control | 22 mm <sup>2</sup> (30%)                              | 4 mm <sup>2</sup> (4%)  |

Table 1: Area and percentage of area required for the camera at its current 256 x 256 format with the 1.2  $\mu$ m HP process ( $\lambda = .6$ ) and scaled to a 1K x 1K format with the scaleable .5  $\mu$ m HP process ( $\lambda = .35$ ).



Original

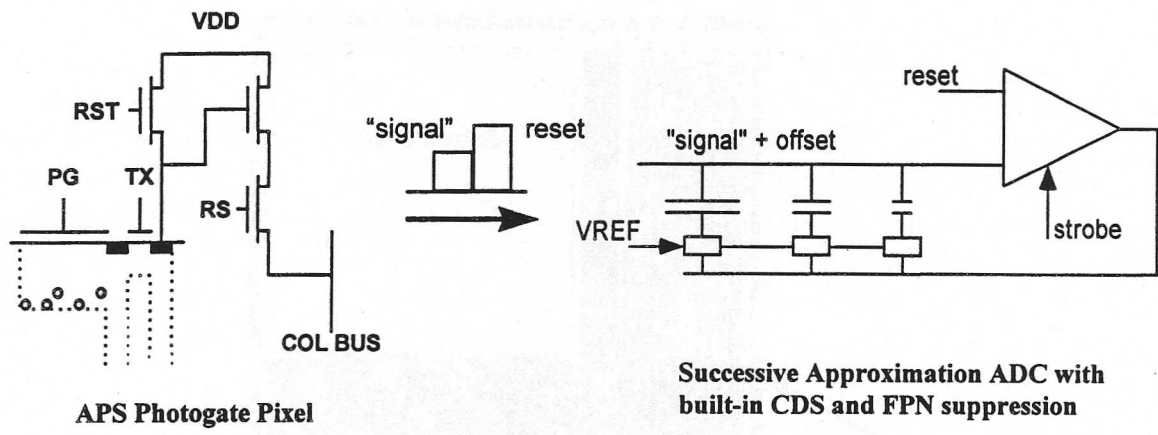


2 x 2 subsampling

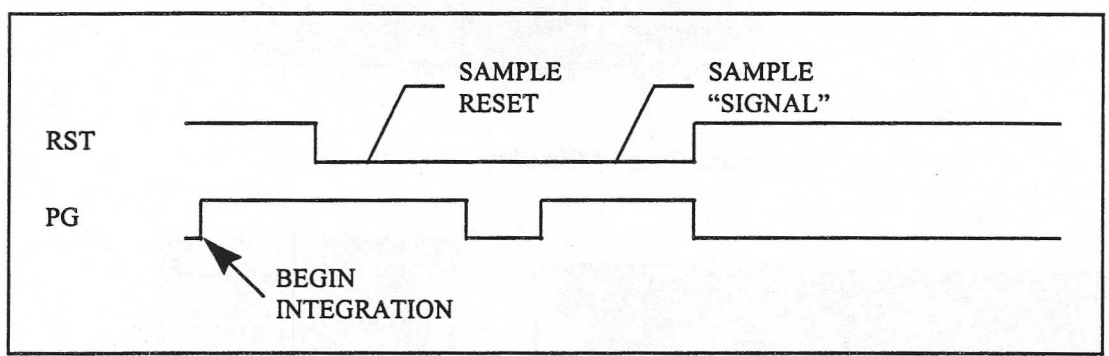


Widow of interest

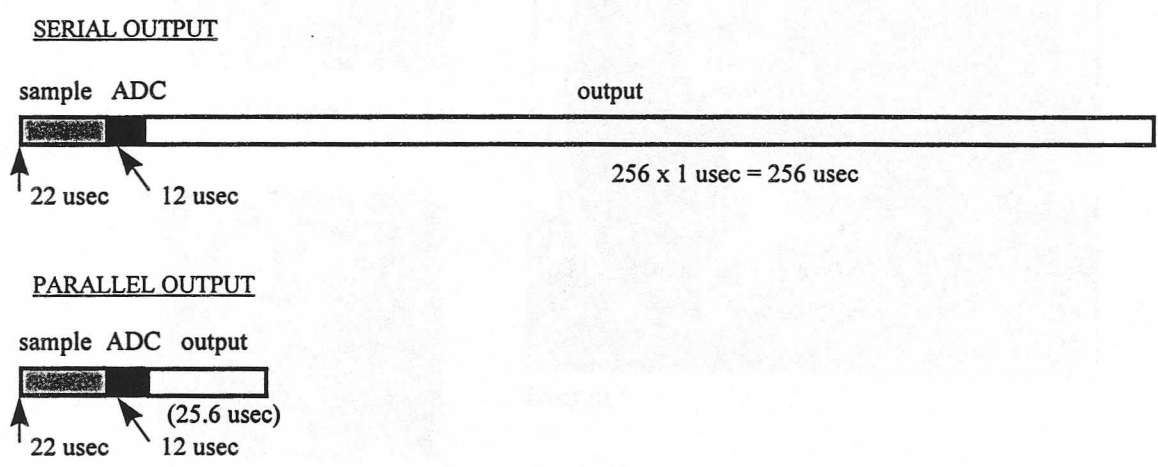
Figure 1: Chip architecture and images taken from the sensor utilizing the different imaging modes.



(a)



(b)



(c)

Figure 2: a) signal chain, b) control signals for photogate pixel operation, c) timing diagram illustrating row read, digital conversion and output for both serial and 10 bit parallel output. With serial output, the time required to read out the data dominates.