256 × 256 CMOS Active Pixel Sensor Camera-on-a-Chip

R. H. Nixon, S. E. Kemeny, B. Pain, C. O. Staller, and E. R. Fossum

Abstract—**A CMOS imaging sensor is described that uses active pixel sensor (APS) technology and permits the integration of the detector array with on-chip timing, control, and signal chain electronics. This sensor technology has been used to implement a CMOS APS camera-on-a-chip. The camera-on-a-chip features a 256 × 256 APS sensor integrated on a CMOS chip with the timing and control circuits, and signal-conditioning to enable random-access, low power (∼5 mW) operation, and low read noise (13 e$^-$ rms). The chip features simple power supplies, fast readout rates, and a digital interface for commanding the sensor, as well as for programming the window-of-interest readout and exposure times. Excellent imaging has been demonstrated with the APS camera-on-a-chip, and the measured performance indicates that this technology will be competitive with charge-coupled devices (CCD's) in many applications.**

I. Introduction

The implementation of the active pixel sensor (APS) camera-on-a chip has great importance for producing imaging systems that can be manufactured with low cost, low power, and with excellent imaging quality. Camera-on-a-chip technology will enhance, or enable, many applications including robotics and machine vision, guidance and navigation, automotive applications, and consumer electronics. Future applications will also include scientific sensors such as those suitable for highly integrated imaging systems used in NASA deep space and planetary spacecraft. The desirable features for all these applications is the integration of support circuitry on the same chip as the focal plane sensor. This is something that is not easily achieved with current charge-coupled device (CCD) technology, but is now possible through the use of standard CMOS processes [1]. The high degree of electronics integration on the focal-plane will enable the simplification and miniaturization of instrument systems, thereby leading to overall lower power and cost. A 128 × 128 photodiode APS version of this chip was developed as a precursor to the work reported here [2].

CCD's are currently the competing incumbent technology for image sensors. However, the CCD technology does not easily lend itself to large scale signal processing. Only limited signal processing operations have been demonstrated with charge domain circuits [3], [4]. Further, CCD's cannot be easily integrated with CMOS without additional fabrication complexity. CCD's are higher capacitance devices resulting in drive electronics that dissipate large power levels for large area arrays. In addition, CCD's require many different voltage levels to ensure high charge transfer efficiency. These limitations can be overcome by the APS [5].

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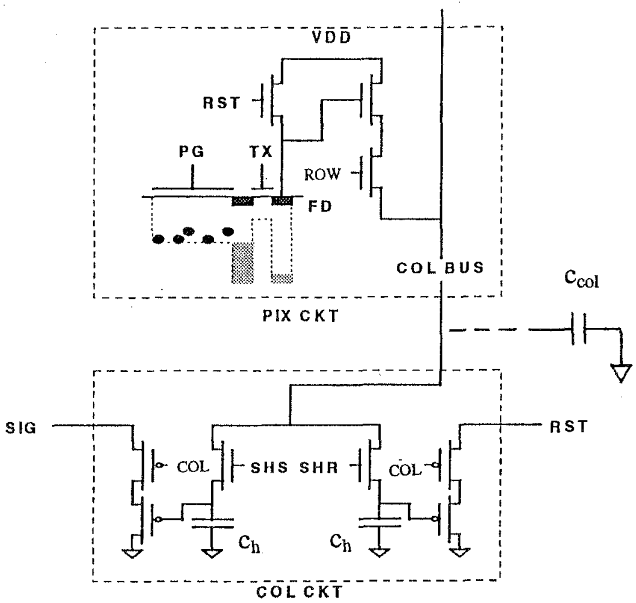

Fig. 1. CMOS APS pixel circui.

The APS camera-on-a-chip features pixels that allow intrapixel charge transfer for correlated double sampling (CDS) [6], and an on-chip double-delta sampling (DDS) for fixed pattern noise (FPN) suppression. These features allow the CMOS APS to achieve low noise performance comparable to a CCD.

The following sections of the paper will first review the basic characteristics of the CMOS APS, followed by a discussion of the design and operation of the chip. In the design section, the timing and control for reading out the array will be presented. Finally, the experimental results based on fabrication and testing will be presented.

II. Basic CMOS Active Pixel Sensor Operation

The operation of the APS sensor has been reported elsewhere [6]. In an APS, both the photo detector and readout amplifier are integrated within the pixel. The voltage or current output from the cell is read out directly through selection transistors rather than using the shift charge technique associated with the CCD. A schematic diagram of a CMOS active pixel circuit is shown in Fig. 1. Incident photons pass through the photogate (PG) and the generated electrons are integrated and stored under PG. The reset and signal levels are read out to separate channels utilizing correlated sampling to reduce kTC noise, $1/f$ noise, and fixed pattern noise from the pixel. Because the CMOS APS pixel utilizes a basic CCD structure in the pixel for charge collection, the performance advantages of the CCD can be preserved.

The sensor is read out in parallel, one row at a time. The signal from the pixel is the difference between the potential on the floating diffusion (FD) node before and after the photo-charges are transferred on it. These two potentials are stored at the bottom of the column capacitors (C_h), by sequentially using the sample-and-hold switches SHS and SHR. The voltages on the capacitors are differentially read out to produce a voltage proportional to the photo-charge. The column capacitors are respectively connected to p-channel source-followers that drive the signal (SIG) and horizontal reset (RST) bus lines. Once the signals from each row are stored on the capacitors, each column is read out successively by turning on column selection p-channel transistors. The column-parallel sampling process typically takes 1–2 μs and occurs in the so-called horizontal blanking interval. Lateral antiblooming is controlled through proper biasing of the reset transistor.

Noise in the sensor is suppressed by the correlated double sampling (CDS) of the pixel output just after reset, before and after signal charge transfer to FD. The CDS suppresses kTC noise from pixel reset, suppresses $1/f$ noise from the in-pixel source follower, and suppresses fixed pattern noise (FPN) originating from pixel-to-pixel variation in source follower threshold voltage. The noise in a CMOS APS is dominated by the white noise from the pixel source follower and the reset noise on the sample and hold capacitors at the bottom of the column. It can be shown that the pixel noise and the sample and hold reset noise can be approximated by

$$\langle v_n^2 \rangle = 2kT\left(\frac{A_{\rm sf}^2}{C_h + C_{\rm col}} + \frac{1}{C_h}\right) \quad (1)$$

where v_n is the voltage noise, $A_{\rm sf}$ is the gain of the pixel source follower, C_h and $C_{\rm col}$ are the sample-and-hold capacitor and the column capacitance, respectively. The factor of two represents the effect of double sampling. The noise expression shown above indicates that the APS noise is governed by the value of the sample and hold capacitance. Typically, this value is between 1–4 pF, and represents a tradeoff between noise, speed, and layout. Additional noise includes that in the broadband column driver circuit. Typical output noise in CMOS APS arrays is of the order of 140–170 μV rms Output-referred conversion gain is typically 7–11 μV/e$^-$, corresponding to noise of the order of 13–25 electrons rms

Quantum efficiency measured in CMOS APS arrays is similar to that for interline CCD's. The power dissipation of an APS array can be very low depending on the desired readout rate. The power associated with readout is primarily determined by the common pixel biasing load on each column and the analog line drivers. The required bias current for a given frame rate (F_r) is determined mainly by the slew requirements on the source-followers. If $C_{\rm col}$ is the capacitance at the bottom of the column, and $C_{\rm load}$ is the capacitance of the line driver, then the average analog power dissipation from the pixel source-follower and the line driver is given by

$$P = 2C_{\rm col}F_rM\Delta V_{\rm col}V_{\rm dd} + 4\alpha C_{\rm load}F_rM\Delta V_{\rm out}V_{\rm dd} \quad (2)$$

where F_r is the frame-rate, M is the total number of pixels readout, $V_{\rm dd}$ is the power supply voltage, $\Delta V_{\rm col}$ is the maximum voltage change at the bottom of the column, $\Delta V_{\rm out}$ is the maximum voltage change at the output of the circuit, and α is a parameter that indicates number of operations per pixel. Typically, the value of α is between 2 and 4, depending upon the extent of signal conditioning used. The first term in the equation shown above is the average power dissipated in the pixel source followers, and the second term is the power dissipated in the subsequent line drivers and buffers. For $M = 256^2$, $C_{\rm col} \sim 2$ pF, $C_{\rm load} \sim 20$ pF, $V_{\rm dd} = 5$ V, $\Delta V_{\rm out} = 1$ V, and $F_r = 30$ Hz, average power dissipation is calculated to be only 2 mW. The power dissipated in the digital timing and control circuits is less than 1 mW, indicating that the integration of the timing and control on-chip can be performed at a minimal focal-plane power penalty. Most importantly, by integrating the timing and control on-chip, the overall system power is vastly reduced by an order of magnitude compared to CCD sensors.

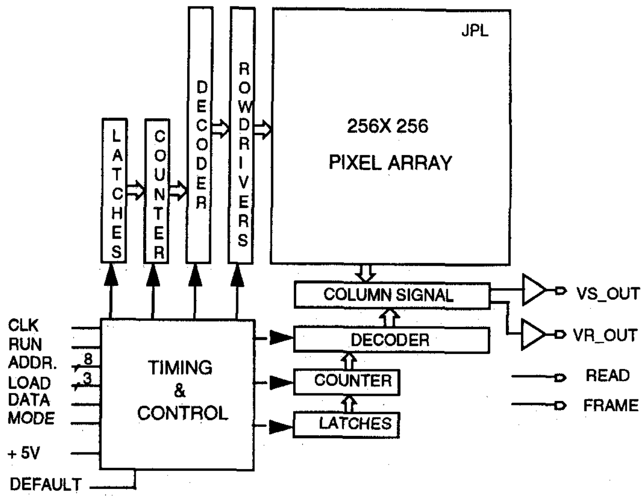

Fig. 2. Block diagram of CMOS APS chip.

III. Chip Design and Operation

A. General

A block diagram of the chip architecture is shown in Fig. 2. The chip inputs that are required are a single +5 V power supply, a start command, and a parallel data load command for defining integration time and windowing parameters. The inputs are asynchronous digital signals; the outputs are differential analog and digital sync. The digital circuits employ common logic elements to control row and address decoders, delay counters, and readout timing.

The chip is programmed to operate with a default window size of 256 × 256. However, the chip can be commanded to

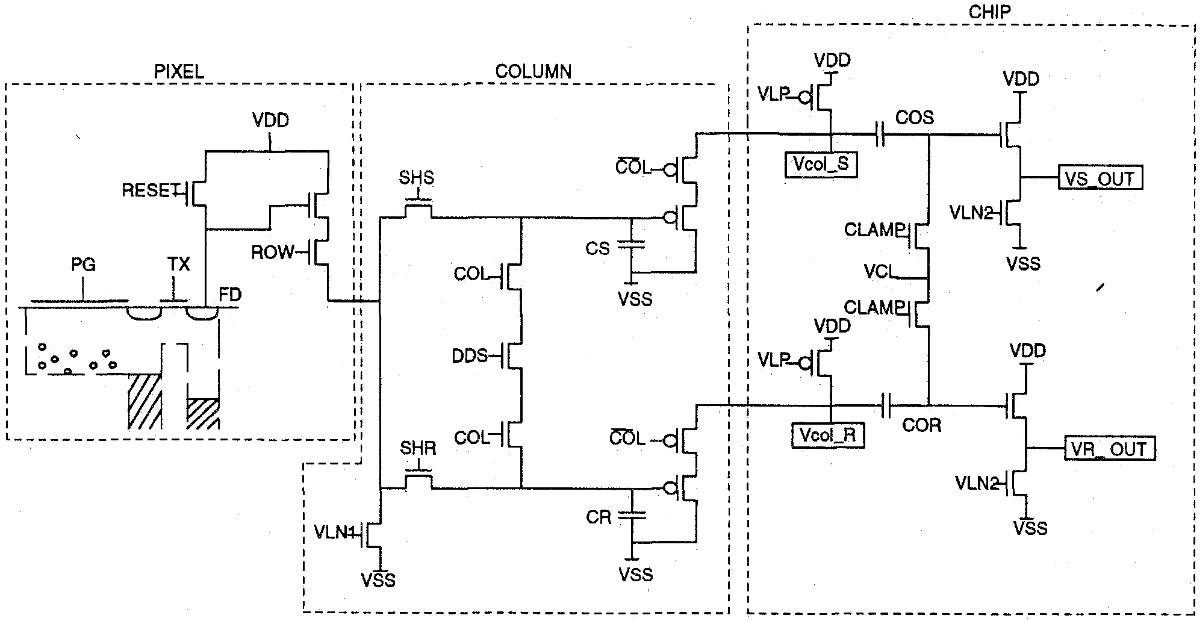

Fig. 3. Schematic of active pixel unit cell and readout circuitry.

read out any area of interest within the 256 × 256 array. This is done by digital commands that preset the decoder counters to start and stop at any value, and are loaded into the chip via the 8-b data bus. A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-b register via the input data bus. A 32-b counter operates from one-fourth the clock input frequency and is preset each frame from the register and so can provide very large integration delays. The input clock can be any frequency up to about 10 MHz. The pixel readout rate is tied to one-fourth the clock rate. Thus, frame rate is determined by the clock frequency, the window settings, and the delay integration time.

B. Readout

The CMOS APS, along with readout circuits, is shown schematically in Fig. 3. The pixel unit cell consists of a photogate (PG), a source-follower input transistor, a row-selection transistor, and a reset transistor. At the bottom of each column of pixels, there is a load transistor and two output branches to store the reset and signal levels. Each branch consists of a 1 pF sample and hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a second source-follower with a column-selection switch (COL). The reset and signal levels are read out separately, allowing correlated double sampling to suppress kTC noise, $1/f$ noise, and fixed pattern noise from the pixel. A double delta sampling (DDS) circuit is used to remove offsets due to the column drivers, and hence reduces column-to-column fixed pattern noise. The DDS circuit calculates the difference between the voltages from two consecutive reads per channel. During the first read, the actual voltage on one of the column capacitors (CR for instance) is read out, and is stored on the coupling capacitor (COR). Following this, the DDS switch is enabled to short the two capacitors CS and CR. The output of the DDS circuit is the difference between the voltage on the capacitor before and after the short. If V_r and V_s are the voltages on the capacitors CR and CS, respectively, before the DDS short, then the output of the chip is given by

$$\text{VS\_OUT} = \gamma(V_{\text{cl}} + \beta\{\alpha[V_s - V_r]/2\} - V_{\text{ts}}) \qquad (3)$$

$$\text{VR\_OUT} = \gamma(V_{\text{cl}} + \beta\{\alpha[V_r - V_s]/2\} - V_{\text{tr}}) \qquad (4)$$

where γ is the gain of the n-channel output driver, β is the gain of the p-channel column drivers, α is the gain of the pixel source follower, V_{cl} is the clamp potential, and V_{tr} and V_{ts} are the threshold voltages of output source followers. It can be seen from (3) and (4) that the resultant output signals are free from any dependence of the individual threshold voltages of the p-channel column drivers, and hence free from column FPN.

The CLAMP switches, the coupling capacitors (COS and COR), and the output drivers are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array. The coupling capacitors COS and COR in the final output stage have a value of approximately 14 pF. These capacitors are kept large to reduce kTC noise and to minimize signal attenuation through the capacitive divider at the final output stage.

The chip can be read out in three different modes. These are photogate, photodiode, and differencing [7]. In the photogate mode each pixel is first reset (RESET) and the reset value is then sampled (SHR) onto the holding capacitor CR. Next, the charge under each photogate is transferred (PG) to the floating diffusion (FD). This is followed by sampling this level (SHS) onto holding capacitor CS. These signals are then placed

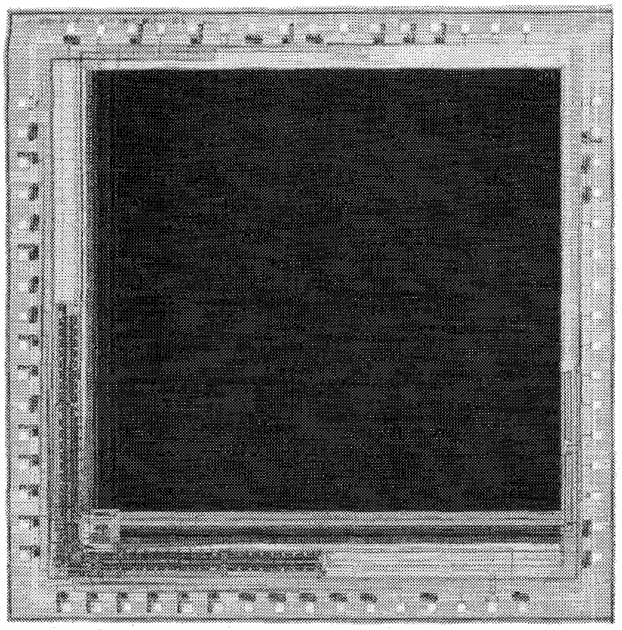

Fig. 4. Chip photograph.

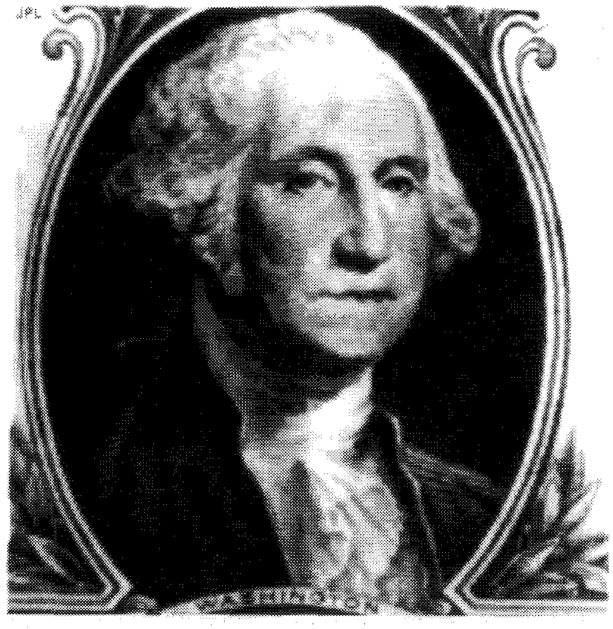

Fig. 5. Sample raw image from sensor.

on the output data bus by the column select circuitry. In the photodiode mode this process is reversed; first the charge under the photogate is read out and then the reset level is sampled. This mode would be used if a photodiode active pixel was substituted in future designs.

In the differencing mode, the capacitors CS and CR are used to store signal from the previous frame and the current frame. This is achieved by altering the timing in the following way: rather than starting with a reset operation, the signal on the floating diffusion is read out to one of the sample and hold capacitors. This represents the previous pixel value. The reset is then performed followed by a normal read operation. This value is then stored on the other sample and hold capacitor. The difference between these two signals is now the frame to frame difference. Note that the current pixel value stored on the floating diffusion is retained until the next frame is ready for read. It then becomes the previous pixel value.

IV. Experimental Results

The chip was processed through MOSIS in the HP 1.2-μm linear capacitor process. Fig. 4 shows a photograph of the chip. A sample image produced for a 256 × 256 window is shown in Fig. 5. Performance was measured for a broad range of parameters. These results are shown in Table I.

The output saturation level of the sensor is 800 mV when operated from a 5 V supply. Saturation is determined by the difference between the reset level on the floating diffusion node (approximately 3 V) and the minimum voltage allowed on the pixel source follower gate (e.g., threshold voltage of approximately 0.8 V plus saturation voltage of the column current sink). This corresponds to a full well of approximately 75 000 electrons. This can be increased by operating at a larger supply voltage, gaining about 47 000 e^- per supply volt.

TABLE I
Performance Characteristics

Parameter	5 Volt Operation	
Saturation Level	800 mV	75,000e-
Conversion Gain	10.6uV/e-	
Read Noise	138 uV	13 e- r.m.s.
Dynamic Range	75 db	5800:1
Peak QE	20-25%	
Fixed Pattern Noise	0.2 % sat p-p	<2mV p-p
Dark Current	29 mV/sec	~500 pA/cm^2
Power	100kpix/sec	~3 mW

Dark current was measured by varying the master clock rate and thus linearly controlling the integration period in the dark. An output-referred, room temperature, dark-current-induced-signal of 29 mV/s was measured. Based on the conversion gain, this yields a dark current of less than 500 pA/cm^2.

Conversion gain ($\mu V/e^-$) was obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. The fixed pattern noise arising from dispersion in conversion gain was under 1%—similar to the value found in CCD's and consistent with the gain of a source-follower buffer amplifier. Output-referred conversion gain was measured to be 10.6 $\mu V/e^-$ which is in reasonable agreement with the estimated photogate pixel parasitic capacitance. The measured quantum efficiency (QE) was found to be similar to a interline CCD, with the peak QE being 25% at 700 nm. The total power consumption of the chip was 3 mW at 100 kpixels/s. The measured power consumption is in excellent agreement with that estimated from (2).

Noise in the chip was measured by sampling a small window at 100 kpixels/s. Smaller window sizes were used in order to suppress dark current noise. Data was acquired with a 16-b analog-to-digital converter card in a PC workstation. Noise was calculated from the variance in the pixel output signal over 1000 frames of data and yielded an input-referred read-noise of 13 e^- rms The measured noise value is consistent with the value predicted in (1). For a 1 pF sample-and-hold capacitor used in this design, the noise from the pixel and sample-and-hold operation amounts to 10 e^- rms, indicating that the noise of the driver circuits have only a minimal impact on the sensor performance.

V. Summary

The design of a CMOS APS chip has been described that integrates the image sensor technology with digital control functions on a single chip. The chip has a single clock and single power supply with a simple digital interface that permits easy restructuring of windows-of-interest and integration times. The measured performance indicates that this technology will produce excellent quality images and is expected to be competitive with CCD's in many applications.

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