On-Chip A/D Conversion for Image Sensors

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ABSTRACT

This paper will discuss on-chip analog-to-digital conversion for image sensors. The paper will first present the rationale for pursuing on-chip A/D conversion. Different approaches to on-chip A/D conversion will be addressed and contrasted. The use of semi-parallel approach using sigma-delta A/D conversion, currently under exploration at JPL using a CMOS active pixel sensor array, will be presented. The design of the image sensor and projected performance parameters will be discussed. The long range goal of a fully digital interface scientific camera-on-a-chip will be described.

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ON-CHIP A/D CONVERSION

Rationale

- Simplify system interfaces and cabling
  - Full digital interface possible - very high system noise rejection
  - Easy, high reliability system design
- Reduce cable count
- Reduce total chip count
- Reduce total system power, mass and volume.
- Possible reduction in focal-plane power dissipation
  - Trade high voltage analog output amplifier power (P=IV) for ADC.
- Eliminate noise introduced by off-chip drive.
- Increase SNR by oversampling techniques.
- Enable additional digital signal processing (DSP) on chip.

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ON-CHIP A/D CONVERSION

Technical Approaches (Summary)

TYPE	# BITS	PWR	AREA	ROBUSTNESS	SPEED
Flash	8-10	High	High	Medium	High
Successive Approximation	10-12	Low	Medium	Low	Medium
Dual-Slope	16	Low	Low	Low	Low
Σ–Δ	18-20	Low	Medium	High	Medium

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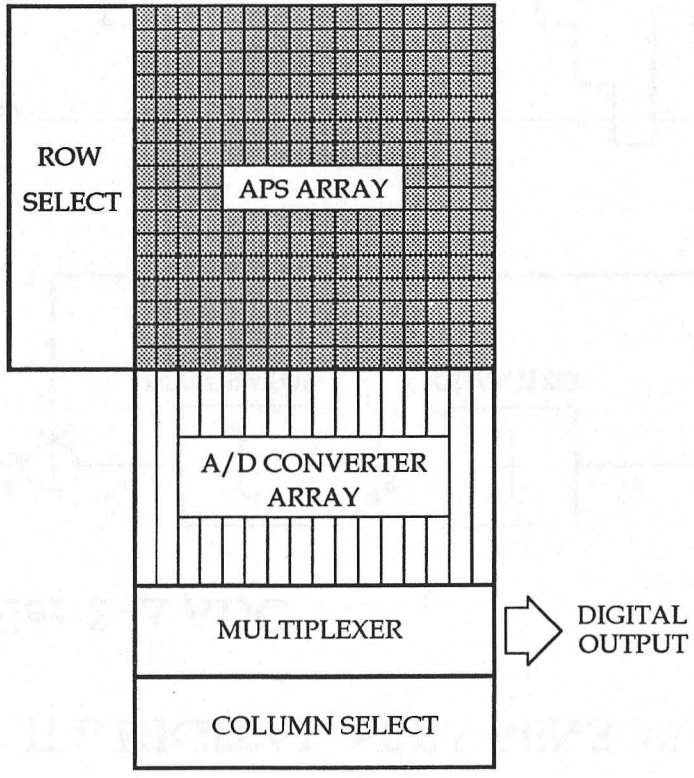
JPL DIGITAL AREA SENSOR

- Column-parallel approach
- Use CMOS APS array



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- Use first order Σ–Δ ADC