CHARGE-COUPLED DEVICES (CCDs)

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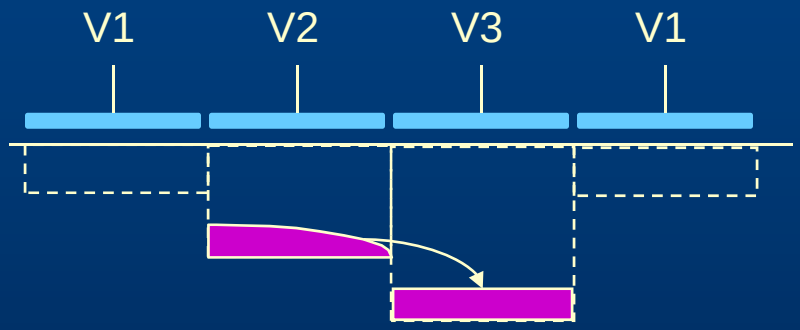
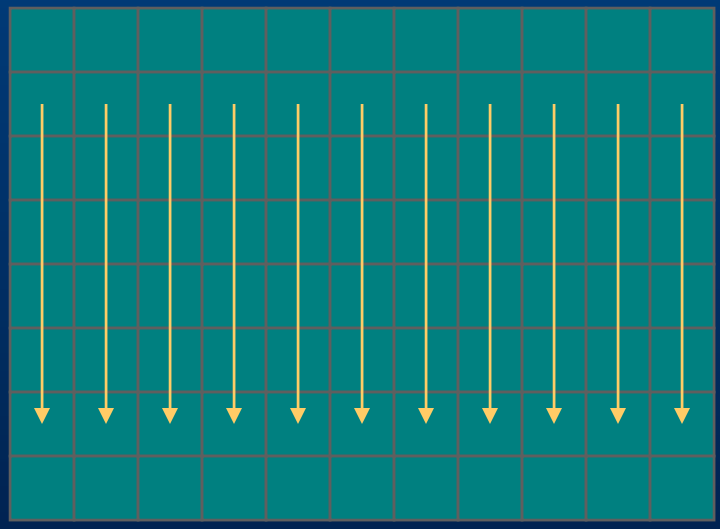
CCD Operation

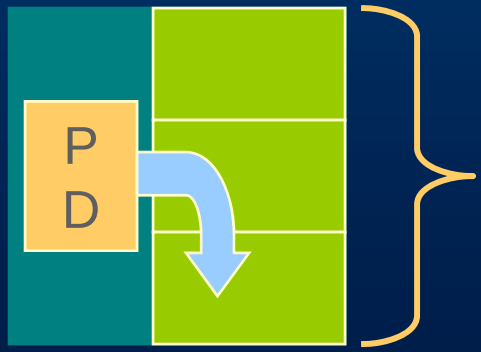
- Charge-coupled devices shift charge one step at a time to a common output amplifier



Parallel vertical shift registers



20% fill factor boosted to 60% with microlens



Horizontal shift register

Amp

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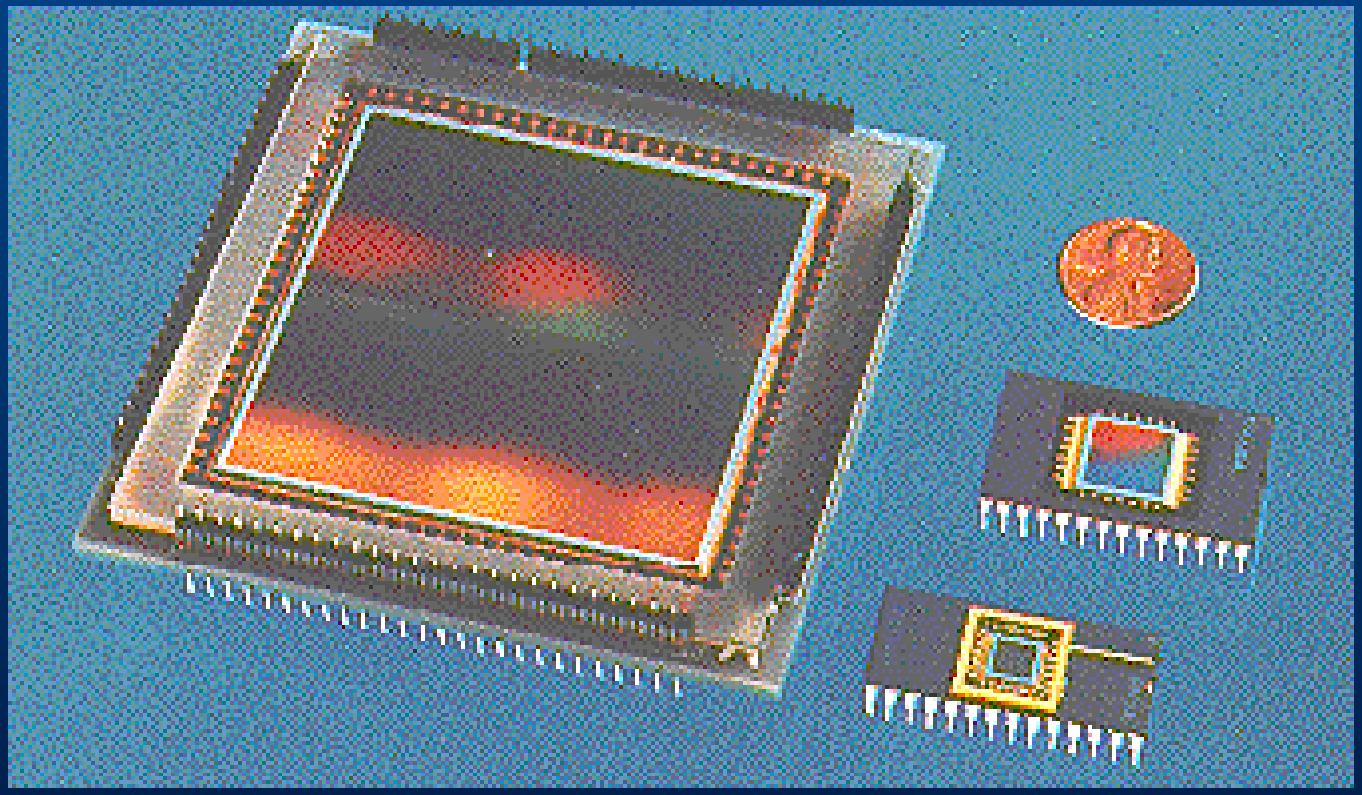
CCDS Are a Mature Technology



- DALSA 25 Mpixel sensor

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CCD Advantages

- Fabrication process tailored for high quantum efficiency
- All charge readout through a single amplifier so no fixed pattern noise (offsets).
- Ability to add charge in charge domain without noise good for some signal processing (e.g. time-delay-integration or TDI scanners).
- Incumbent technology (over 30 years of development)

CCD Limitations

- Requires high charge transfer efficiency
  - Special fabrication process adds cost
  - Larger voltage swings, different voltage levels
- Difficult to integrate on-chip timing, control, drive and signal chain electronics
  - Process integration increases cost, reduces yield
  - Large capacitances require high current levels
- Requires timing generator chip, driver chips, signal processor, ADC and interface chips
- System power in 0.5-2 Watt range
- Architecture yields serial access to image data

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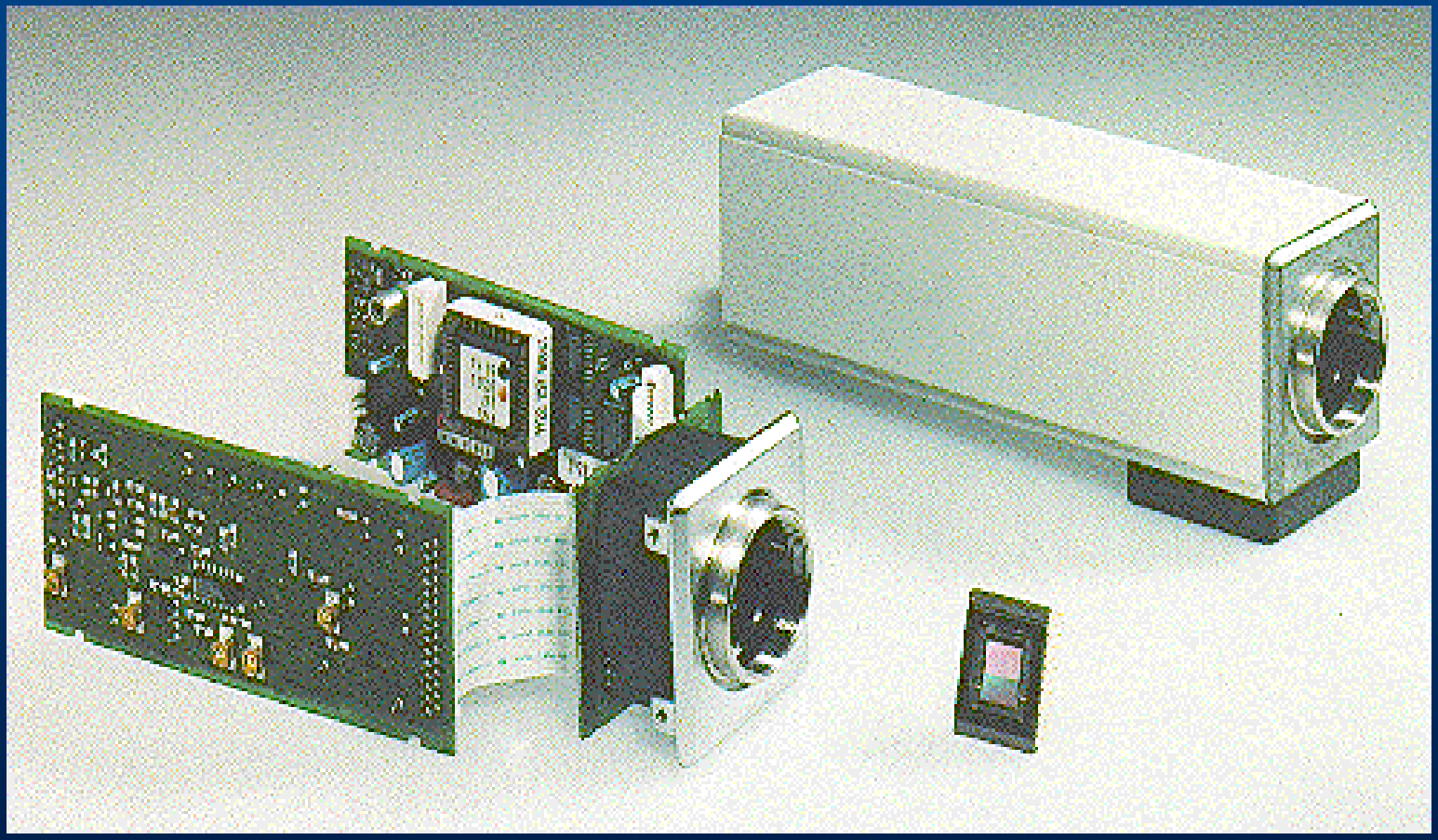
Total CCD Camera Power is High



- CCD imaging systems require many off-chip components

CMOS IMAGE SENSOR HISTORY

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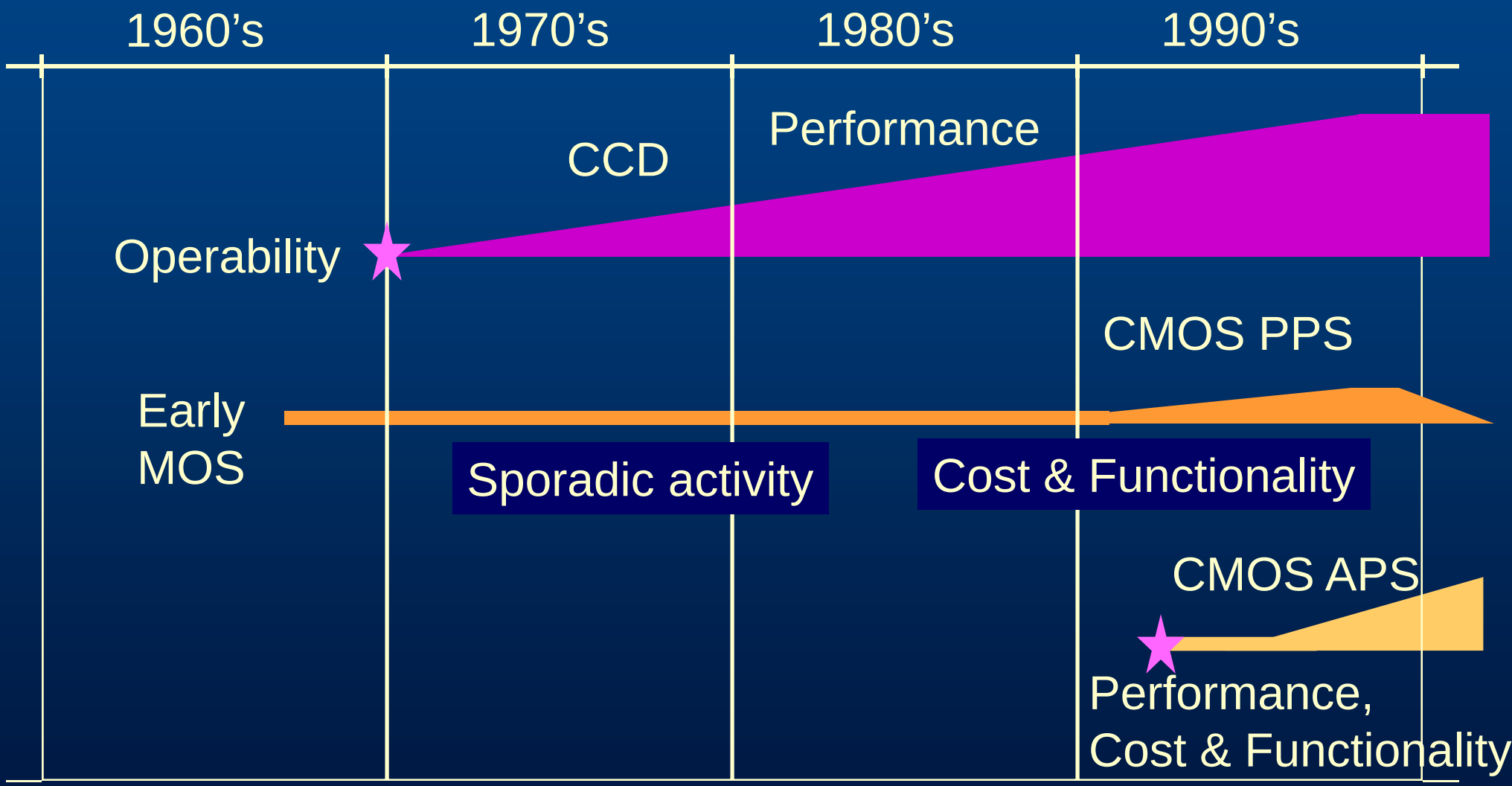
TIMELINE



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Short History of CMOS Image Sensors

- 1960's — Early work on MOS imaging devices
  - *They don't work too well due to state of the art of MOS*
- 1970's — CCDs work better than MOS devices
- 1980's — Limited work on MOS/CCD imagers
- 1990's — CMOS passive pixels commercialized, low performance
- 1993 — First CMOS APS demonstrated (28x28) by JPL
- 1994 — CMOS APS performance comparable to CCDs
- 1995 — CMOS APS as large as 1Kx1K demonstrated
  - *Photobit formed by JPL team to commercialize CMOS APS*
- 1996 — Photobit demonstrates high performance CMOS APS with on-chip ADC at video rates
- 1997 — Photobit reports world's first high performance digital camera-on-a-chip (Stanford Hot Chips Symposium)

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Technology Acceptance

1991

- VVL PPS from U. Edinburgh
- IVP PPS from Linkoping Univ.
- NHK CMOS
- CMD at Olympus
- BCMD at TI

1992

- Active pixels for NASA
- Trip to Japan sparks no interest in camera-on-a-chip -- “CCDs forever”
- CMOS APS invented at JPL

1993

- First 28x28 CMOS APS demonstrated
- No interest at 1993 IEEE Workshop on CCDs/AIS

1994

JPL signs Tech Transfer to Kodak, AT&T

1995

- Business Week article
- Photobit formed
- Rockwell visits JPL
- JPL transfers tech to National

1996

- Kodak signs Photobit as design house, Moto as fab
- Photobit does designs for computer chip company, Lucent, ITT, others
- Toshiba, Hyundai, Intel start CMOS APS efforts
- Polaroid teams with Atmel
- TI offers “CMOS” APS

1997

- VVL, Omnivision switch to APS
- DALSA teams for CMOS APS
- Moto starts “independent” effort
- Smaller companies jump in

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Timing Is Everything

- CMOS state of the art is ripe for image sensors
  - Design rules permit competitive pixel sizes
  - Defects and contamination well controlled
  - Threshold voltages stable and fairly uniform
  - And now foundries offer specialized image sensor modules
- Customers demand low power, miniaturized systems-on-a-chip
- Circuit techniques developed for high performance
  - Active pixel provides gain in pixel and lower noise
  - Use of double-correlated sampling and double-delta sampling on-chip removes temporal & fixed pattern noise
  - Column parallel architecture permits low analog bandwidths to reduce noise and artifacts and maintain high frame rate.
  - Low power imaging circuit techniques reduce power to mW levels

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Advantages over CCDS

- *CMOS Camera-on-a-chip technology is better than CCDs because:*
  - Much lower power - important for portable applications
  - System-on-a-chip integration allows smaller cameras
  - Lower cost of sensor chip and fewer components in camera
  - Easy digital interface for faster camera design & time to market
  - Less image artifacts - no blooming or smear, with same sensitivity
  - Higher dynamic range for security and auto applications
  - Digital output for faster readout speeds and frame rates
  - Direct addressing of pixels allows electronic pan/tilt/zoom
  - Faster design cycles means faster evolution path