CCDs,Smart Sensors, CMOS Image Sensors, and Photon-Counting Quanta Image Sensors – A walk in the past and possibly into the future.

Eric R. Fossum

Sony, Oslo, Norway

November 18, 2025

1982

1995

2025

DARTMOUTH

CMOS Image Sensor (CIS) Invention and Development and the Quanta Image Sensor (QIS)

Eric R. Fossum

Optica NE Section

Optikos, Wakefield, MA

November 20, 2025

DARTMOUTH

ON
QC
WA
MT
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MI
OR
ID
SD
WY
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Cuba
Puerto Rico
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NY
MA
PA
MD
DE
WV
VA
PE
NS
VT
Dartmouth
Harvard
Cornell
MA
RI
Brown
CT
Yale
NJ
Columbia
Princeton
Penn
OH

MOS "Photomatrices"
A zeroth generation image sensor

Mid 1965

Gene Weckler
Fairchild with Rudy Dyck
and startup Reticon

First photo-integration on PN Jnc Cap

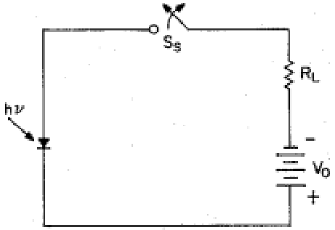


Fig. 1. An idealized circuit for analyzing storage mode operation of a *p-n* junction diode.

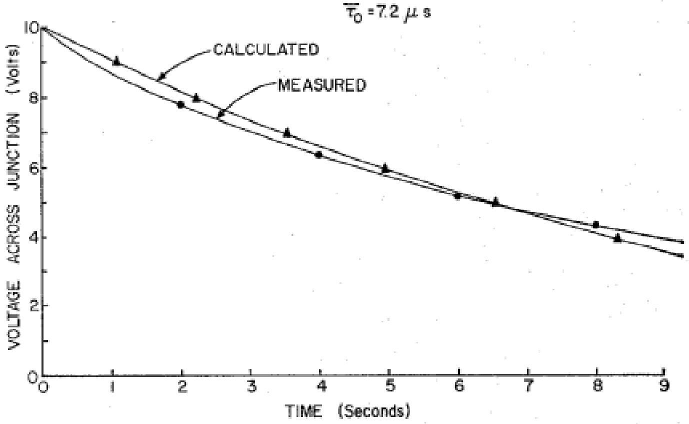
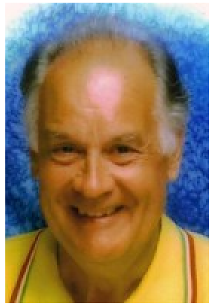
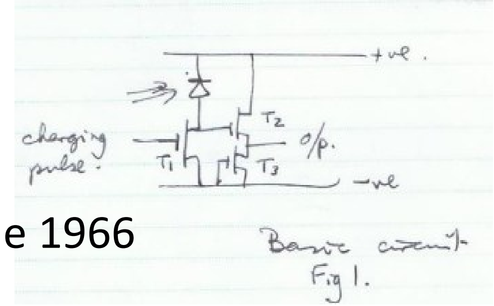


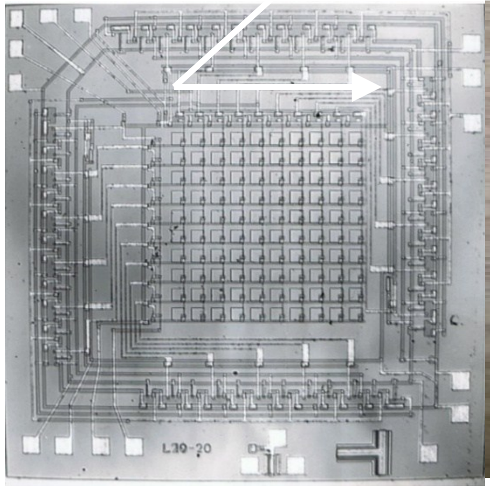
Fig. 2. Measured and calculated voltage decay characteristics of an open-circuited reverse-biased *p-n* junction with zero incident illumination.

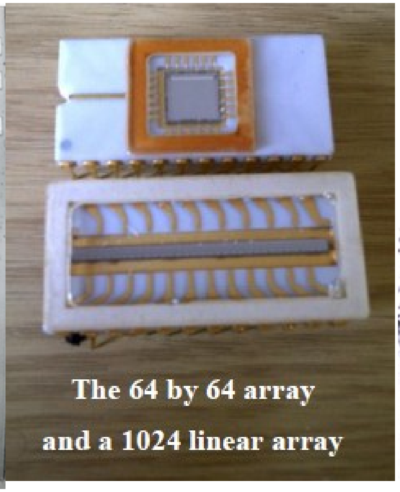


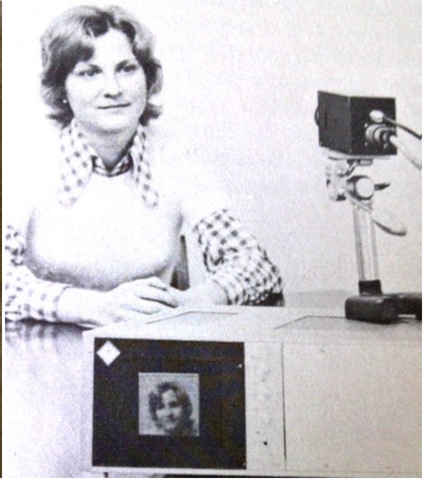
~June 1966



First self-scanned →
Sensor 10x10 1966/67







Peter JW Noble

Mid-late 1960's
MOS arrays at Plessey
with startup Integrated Photomatrix Ltd. (IPL)

Charge-Coupled Device (CCD)

- CCD invented at Bell Labs 1969 (Boyle/Smith
- Practical CCD image sensor at Bell Labs 1970 (Tompsett).
- Interline transfer (ILT) CCD Fairchild 1973 (Amelio, Walsh, Dyck)

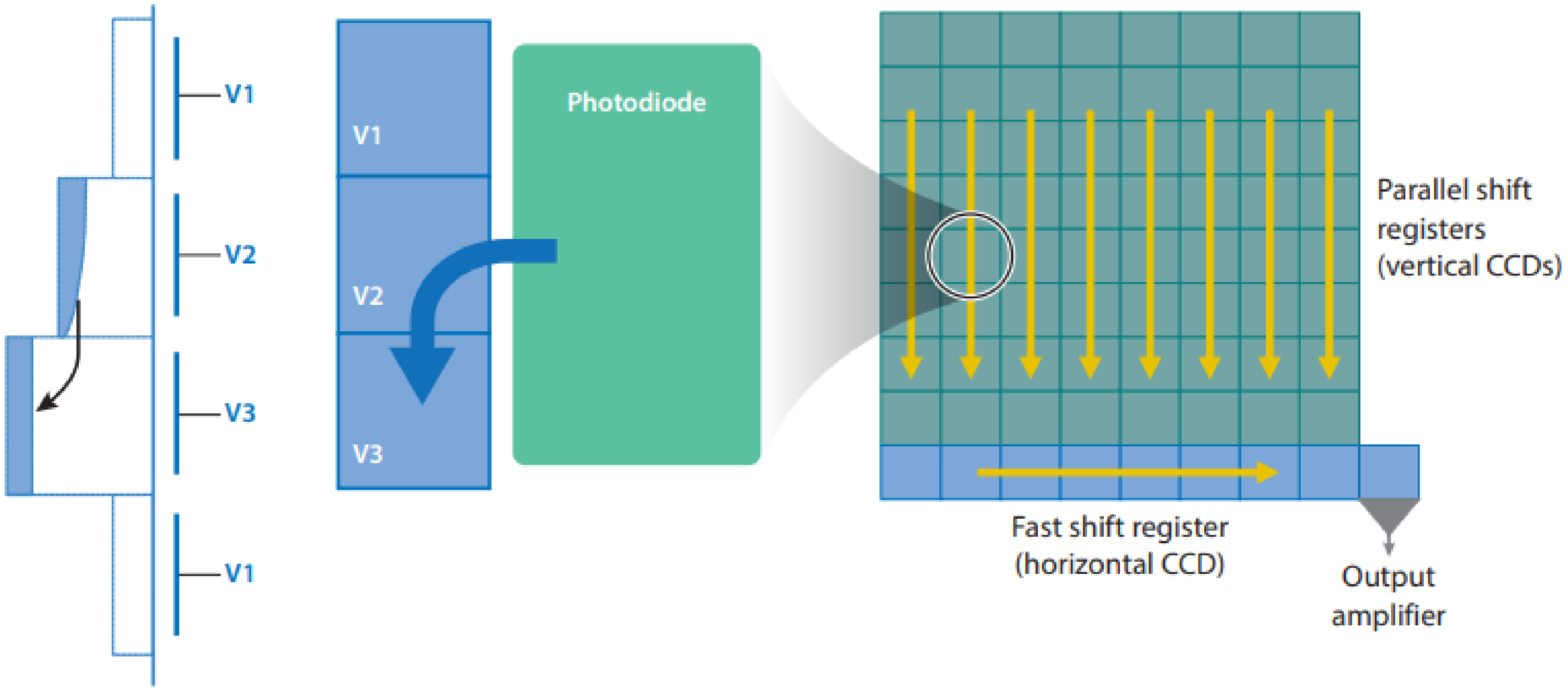


Photo: U. Montan
Willard S. Boyle

Photo: U. Montan
George E. Smith

Michael F. Tompsett

Circa Spring 1970.
What was Eric doing 55 years ago ?

Eric Fossum (left) tracking weather balloons at the
Talcott Mountain Science Center, Avon, CT USA

DARTMOUTH

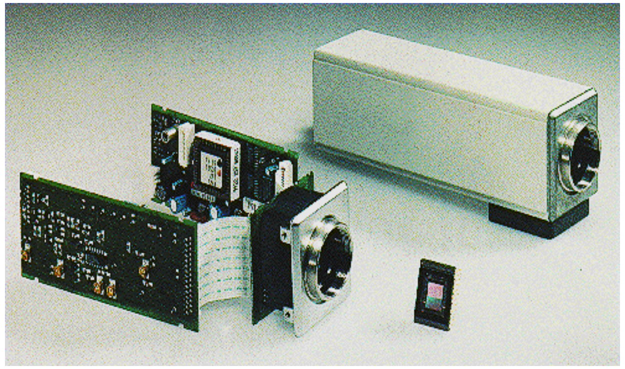
CCD Cameras 1970’s - 1990’s

Early 70’s Bell Labs CCD camera by Mike Tompsett et al.

Steve Sasson with first Kodak self-contained digital camera (1975)

NASA Galileo Spacecraft CCD camera (with optics) early ’80s (800x800)

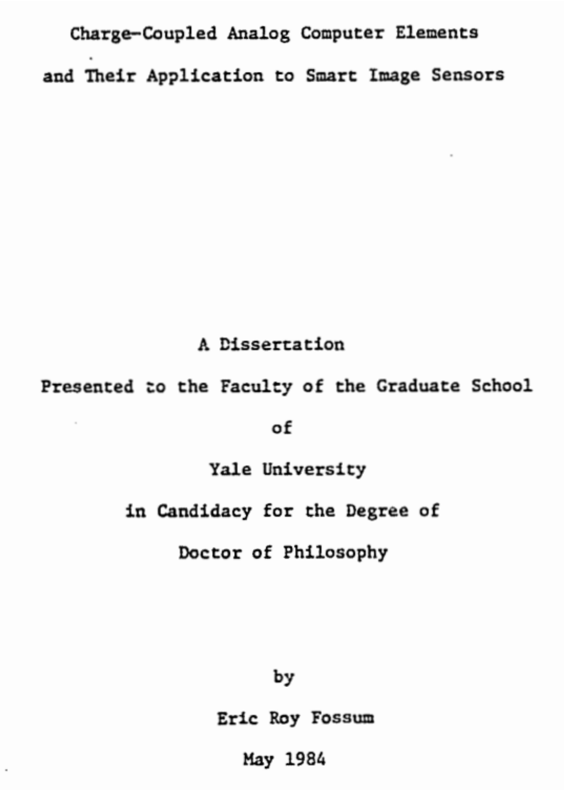
RCA Camcorder



DALSA industrial CCD camera late ’80’s

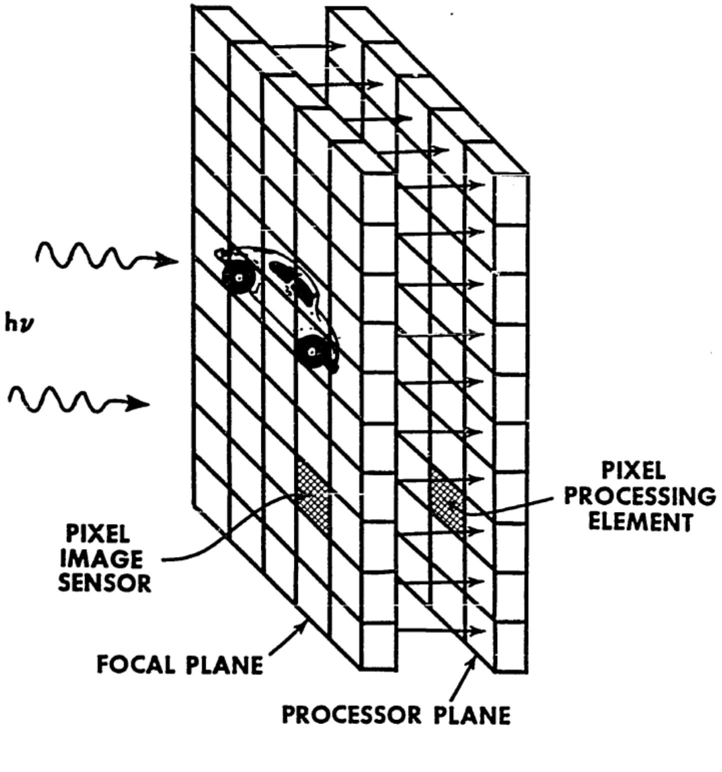
Sony Camcorder early 90’s

“Smart Image Sensors” ~1980-1984
(now “edge computing”)


Charge-Coupled Analog Computer Elements
and Their Application to Smart Image Sensors

A Dissertation
Presented to the Faculty of the Graduate School
of
Yale University
in Candidacy for the Degree of
Doctor of Philosophy

by
Eric Roy Fossum
May 1984



2.1-1 Schematic illustration of focal plane image processing.

Charge-domain analog computing devices for discrete-time focal-plane image processing.

E.R. Fossum, Charge-Coupled Analog Computing Elements and Their Application to Smart Image Sensors, Ph.D. Thesis, Yale University, Department of Electrical Engineering, 1984

Charge-Coupled Computer

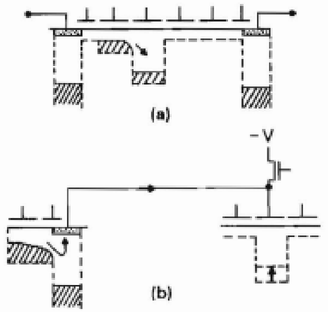


Fig. 1. Illustration of three-dimensional charge coupling. (a) Conventional lateral coupling for charge transfer. (b) 3-D coupling using gate charge subtraction. The circuit operation is described in the text.

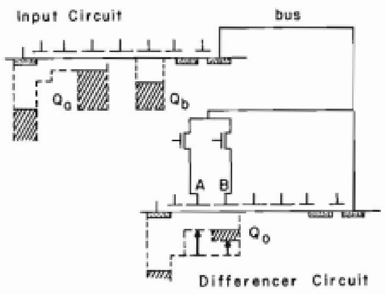


Fig. 2. Linear charge-packet-differencing circuit. Charge packets Q_a and Q_b are subtracted from the gate charge on electrodes A and B, respectively. The operation is discussed in detail in Ref. 6.

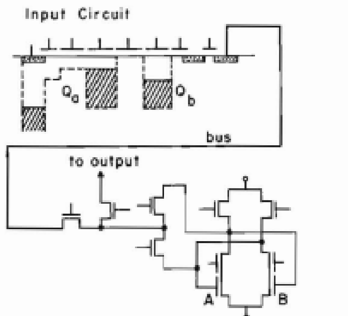


Fig. 3. Charge-packet-magnitude comparator. Charge packets Q_a and Q_b are used to preset node voltages A and B, respectively, of balanced flip-flop.

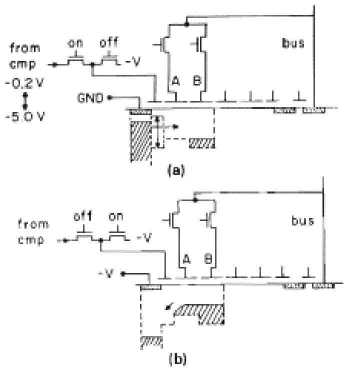


Fig. 4. Gated charge-packet differencer. The input transfer gate is used to conditionally block the fill cycle of the differencer.

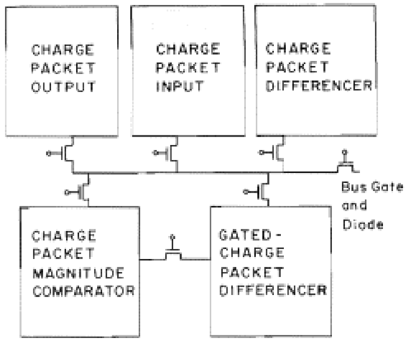


Fig. 5. Block diagram of architecture of the prototype charge-coupled computer.

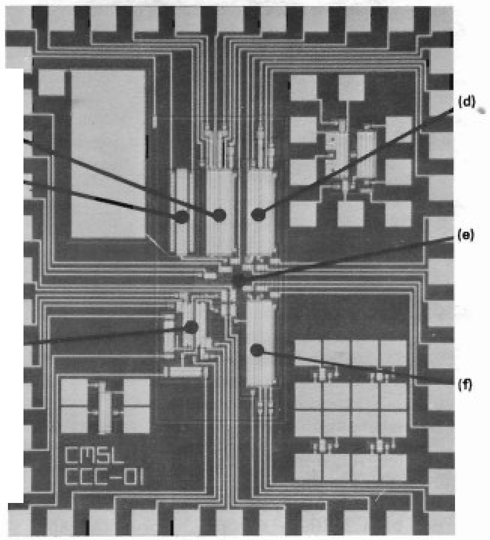


Fig. 6. Photograph of fabricated prototype charge-coupled computer. Wiring is 10 μm in width. Chip size is 2.2 × 2.6 mm. (a) Input. (b) Output. (c) Magnitude comparator. (d) Regular differencer. (e) Bus. (f) Gated differencer.

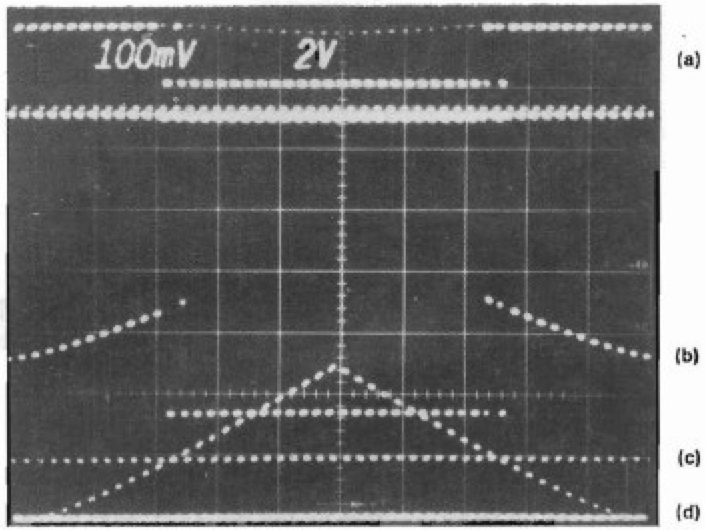


Fig. 13. Output of gated charge-packet differencer as controlled by charge-packet-magnitude comparator. (a) Comparator output. (b) Output. (c) Input A. (d) Input B.

E.R. Fossum, *Charge-Coupled Computing for Focal Plane Image Preprocessing*, Opt. Eng., 26 (9), pp. 916-922, 1987.

Wire-Transfer CCD

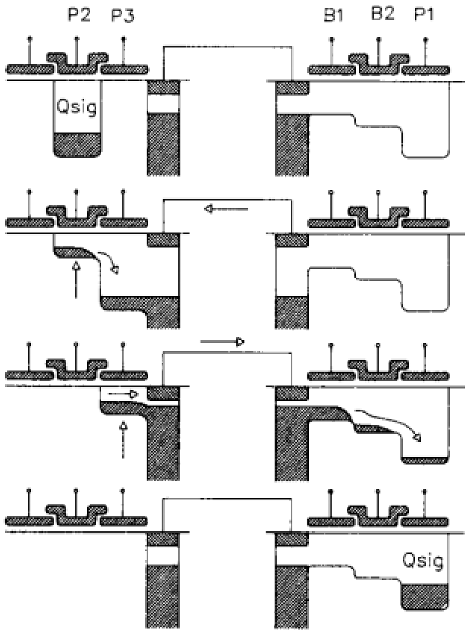


Fig. 1. Illustration of the wire-transfer process.

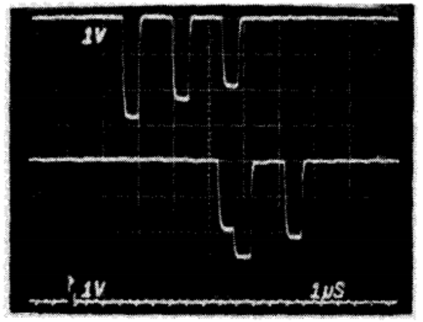


Fig. 11. Double-exposure photograph showing output of shift register following parallel load of 3 charge packets (top trace) and following load and recirculation of first packet (second trace). Lower trace shows voltage pulse for generating charge packet.

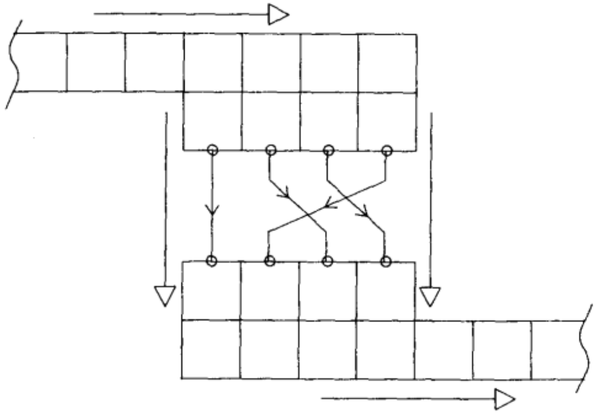
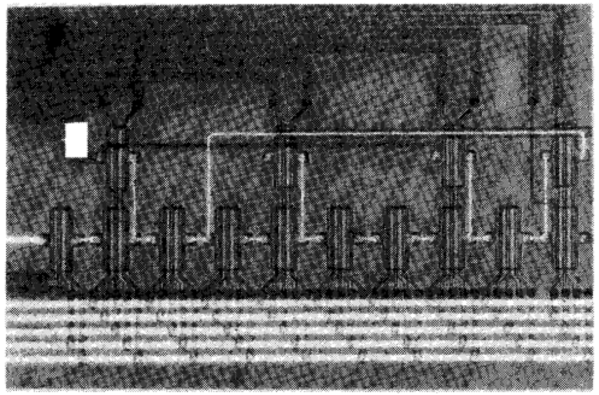
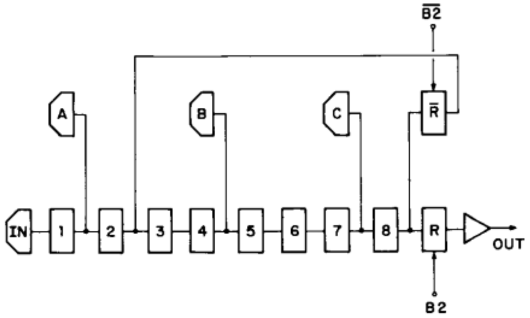


Fig. 12. Block diagram of serial/parallel-parallel/serial circuit for arbitrary reordering of serial charge packet data stream using wire transfer.



(a)



(b)

Fig. 9. (a) Photograph of router/parallel-load experiment. (b) Block diagram of router/parallel-load experiment.

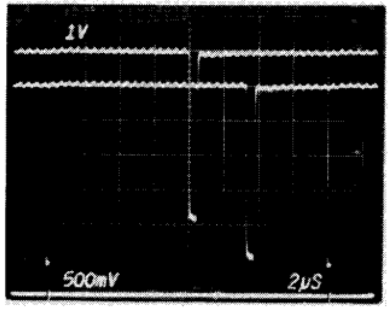
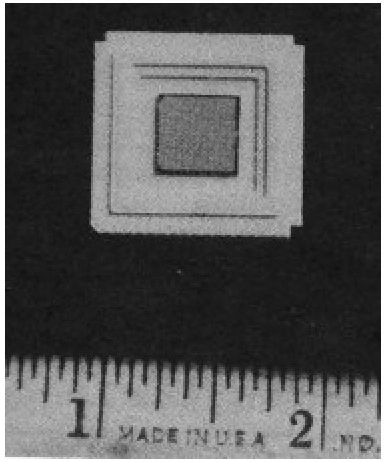


Fig. 10. Double-exposure photograph showing output of shift register for one programmed loop (top trace) and two loops (second trace). Lower trace shows voltage pulse for generating charge packet.

E.R. Fossum, *Wire Transfer of Charge Packets Using a CCD-BBD Structure for Charge-Domain Signal Processing*, IEEE Trans. Electron Devices, vol. ED-38(2) pp.291-298, 1991

Focal-Plane Image Processor: 1989
(48x48 Pixels and Processors)



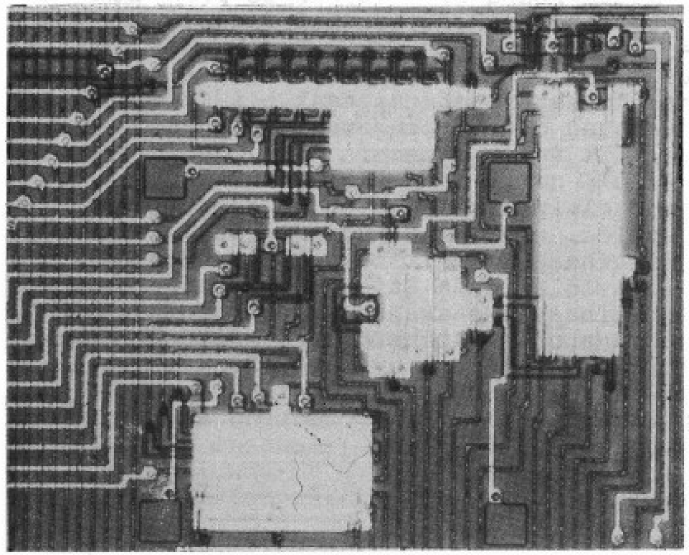


Fig. 3. IRET unit cell (360 X 360 um^2).

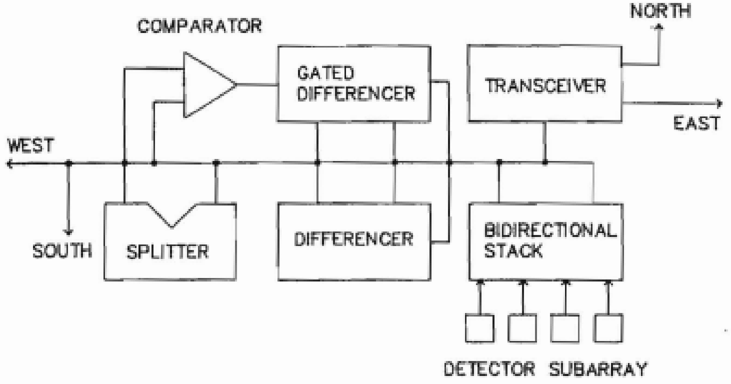
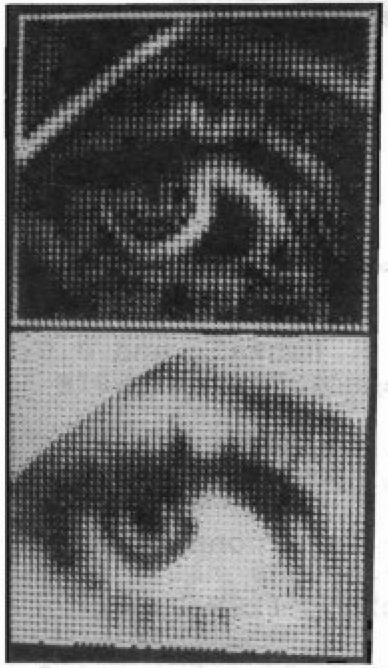


Fig. 2. Block diagram of the unit cell.

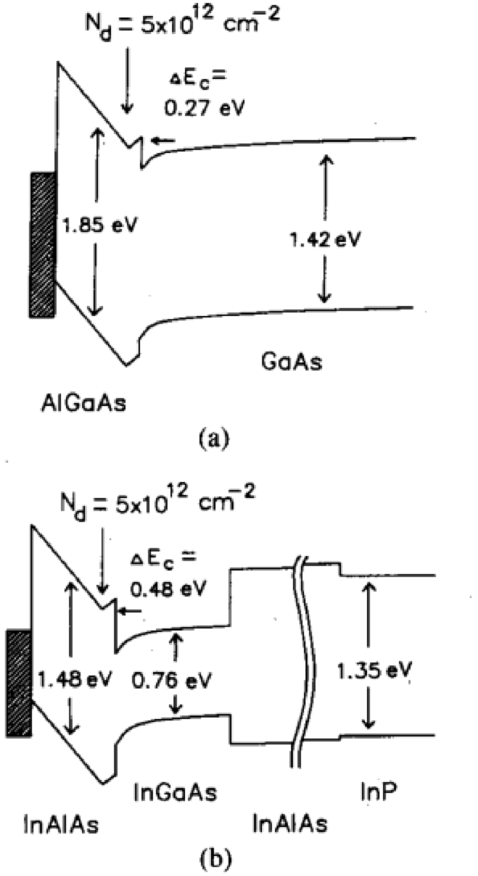


E-S. Eid and E.R. Fossum, *Real-Time Focal-Plane Array Image Processor*, Proc. SPIE vol. 1197, pp. 2-12, 1989.

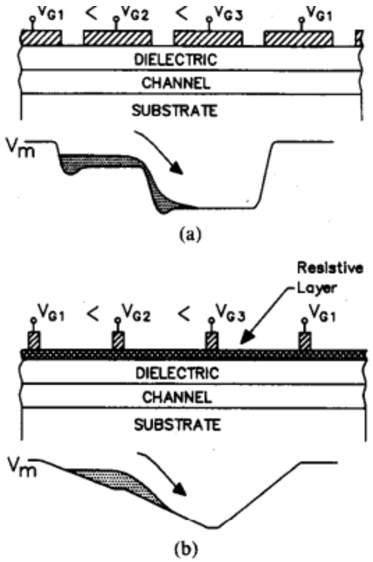
IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 5, MAY 1991

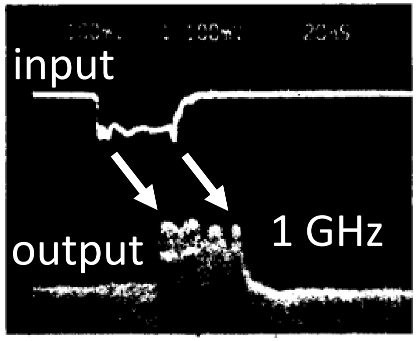
Two-Dimensional Electron Gas Charge-Coupled Devices (2DEG-CCD's)

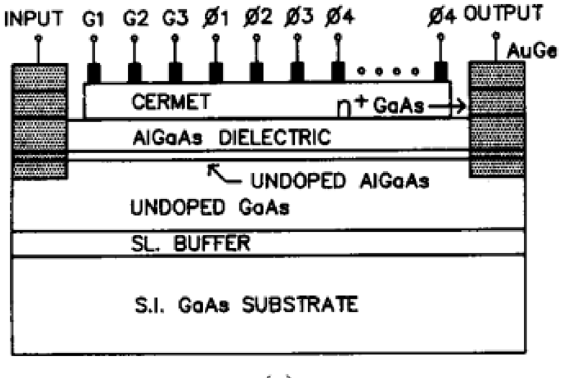
Eric R. Fossum, *Senior Member, IEEE*, Jong-In Song, and David V. Rossi, *Student Member, IEEE*



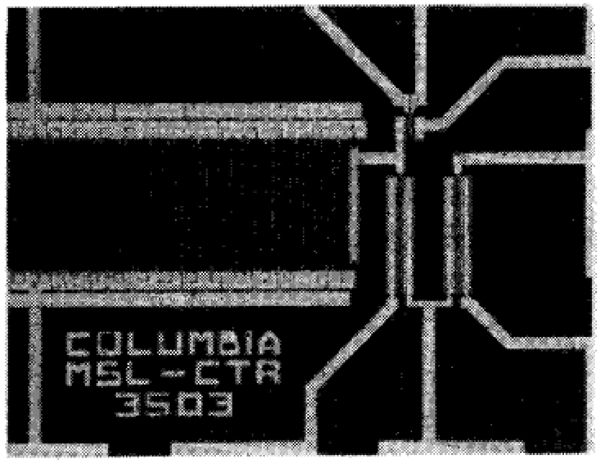
Band diagrams for (a) $Al_{0.3}Ga_{0.7}As$/GaAs material system and (b) $In_{0.52}Al_{0.48}As$/$In_{0.53}Ga_{0.47}As$/InP material system.





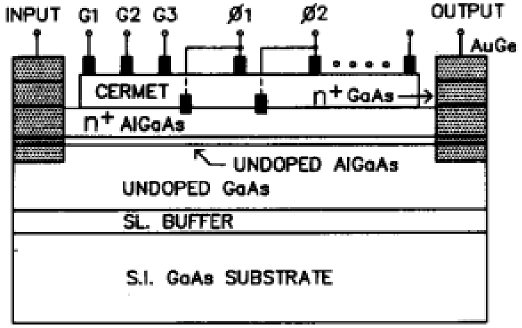


(a)

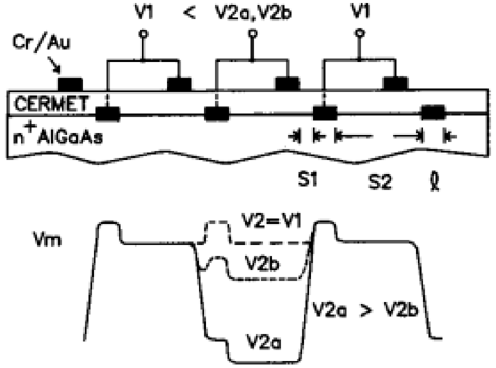


(b)

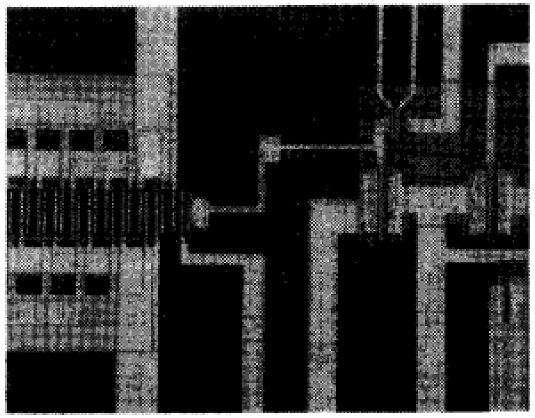
A four-phase, resistive-gate 2DEG-CCD delay line. (a) (



(a)



(b)



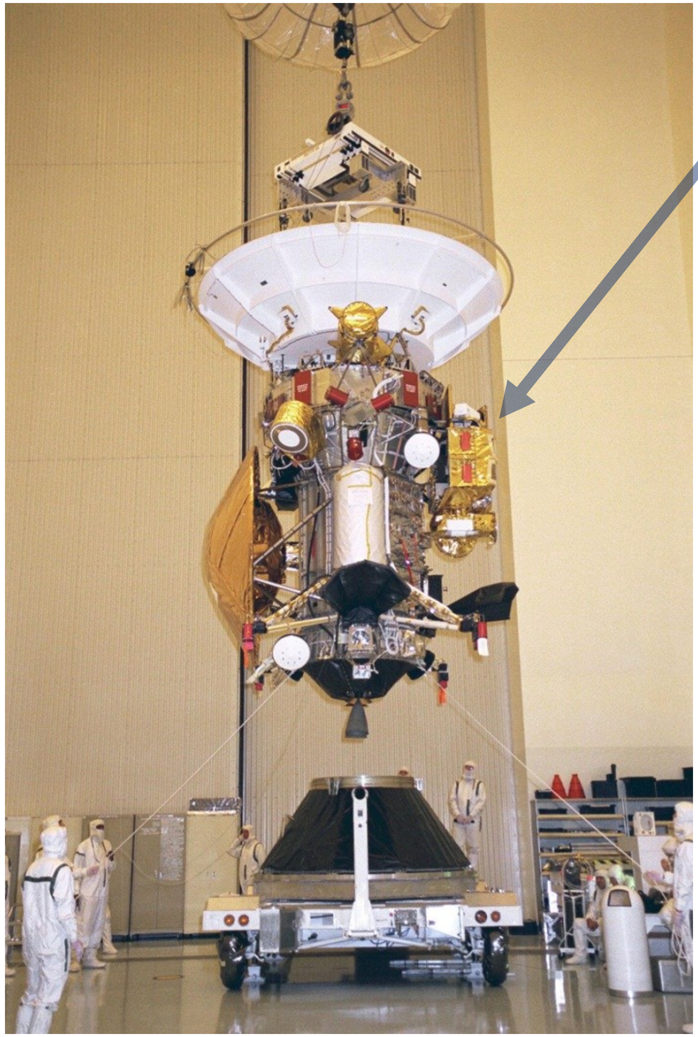
(c)

Fig. 11. A two-phase, resistive-gate 2DEG-CCD delay line. (a) Material layers. (b) Electrode configuration and resultant potential wells (l = 2 μm, s_1 = 1.5 μm, s_2 = 6.5 μm). (c) Chip photograph.

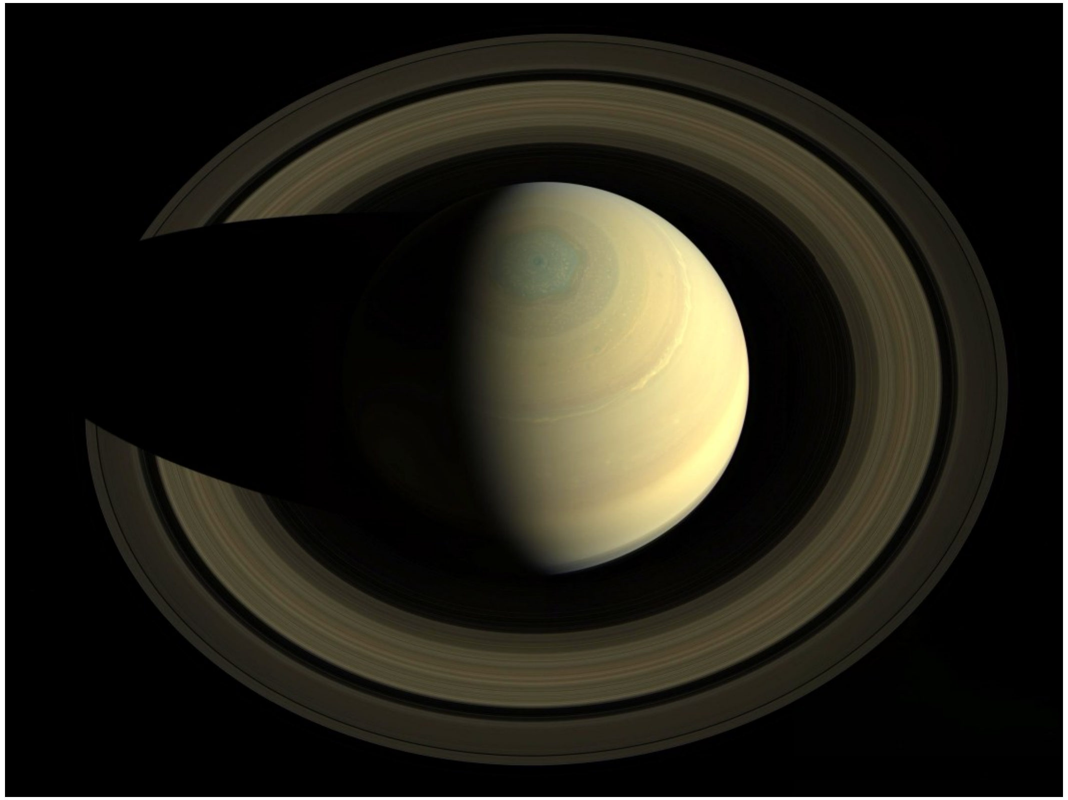
Conclusions to Preamble

- Analog signal processing is hard. Especially when you have to invent stuff along the way.
- Took nearly 10 years to get from concept to demonstration.
- A few analog designers are a lot slower at making progress than a few thousand digital designers (or ten-thousand coders).
- New materials + devices fun, but hard to get acceptance unless compelling. Also, many many unexpected issues.
- Maybe the best thing to do was to stay with silicon and get the ADC onto the CCD chip so we could then do focal-plane image processing in digital on or near the focal plane.

1990's NASA needs smaller cameras for smaller interplanetary spacecraft



Cassini CCD camera

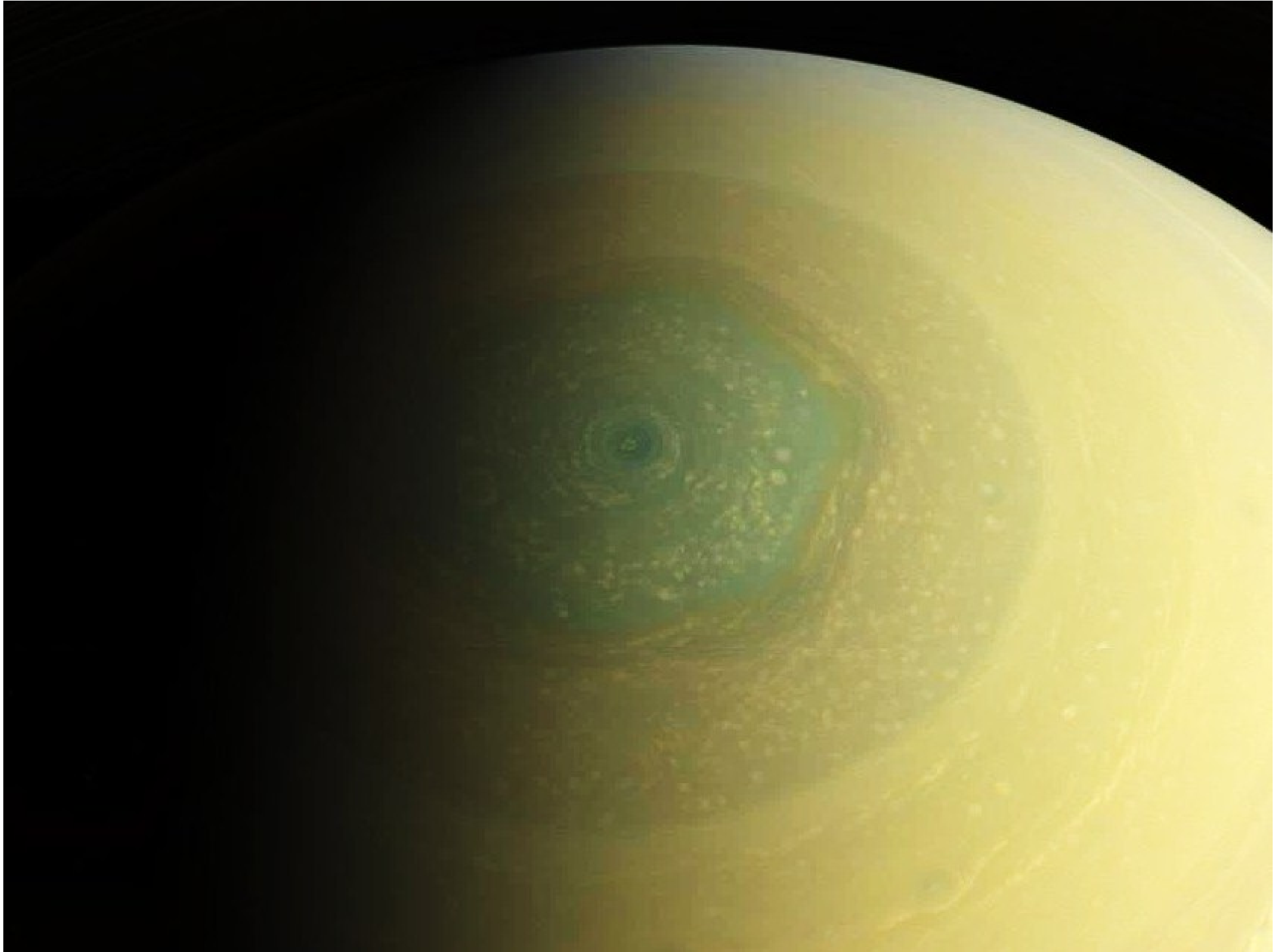


https://photojournal.jpl.nasa.gov/catalog/PIA17474

Saturn from above

Jet Propulsion Laboratory
California Institute of Technology

Jet Propulsion Laboratory



Feb 1993 -- Active Pixel Sensors: Are CCDs Dinosaurs?

Charge transfer is Achilles heel of CCD

- Radiation impact on CCD charge transfer efficiency
- High voltages needed for CCD charge transfer
- Impact of temperature on CCD operation
- Slow readout rate
- Serial access to data
- Requires lots of support electronics to drive CCD and read out CCD

Integration is well-known path to miniaturization

- CMOS not easy to integrate with large area CCD
- Use best performing aspects of CCD
  - Pinned-photodiode detector
  - Complete charge transfer
  - Floating-diffusion output amplifier
  - Correlated double sampling
- Additional fixed pattern noise suppression circuits
- On-chip ADC

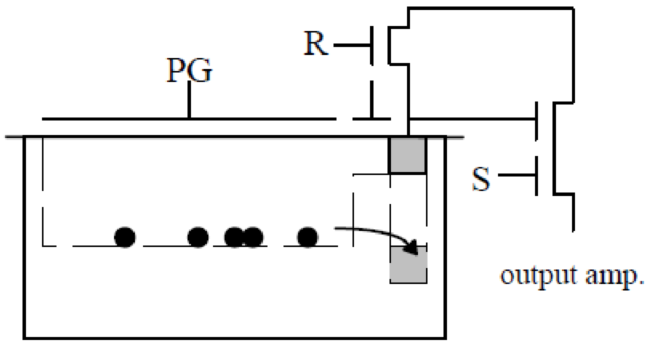


Fig.2. Schematic of a simple, CMOS-compatible active pixel.

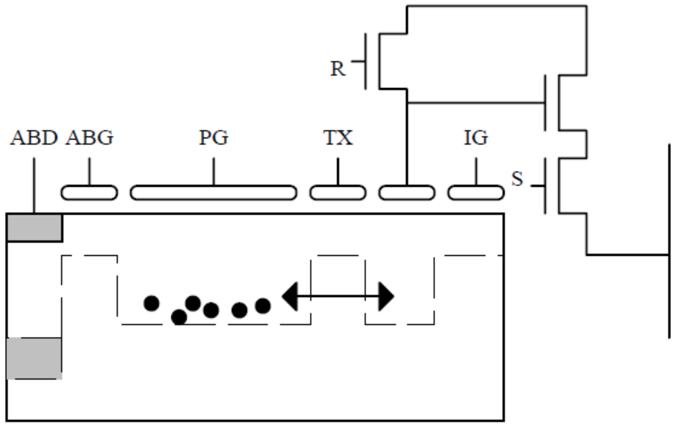
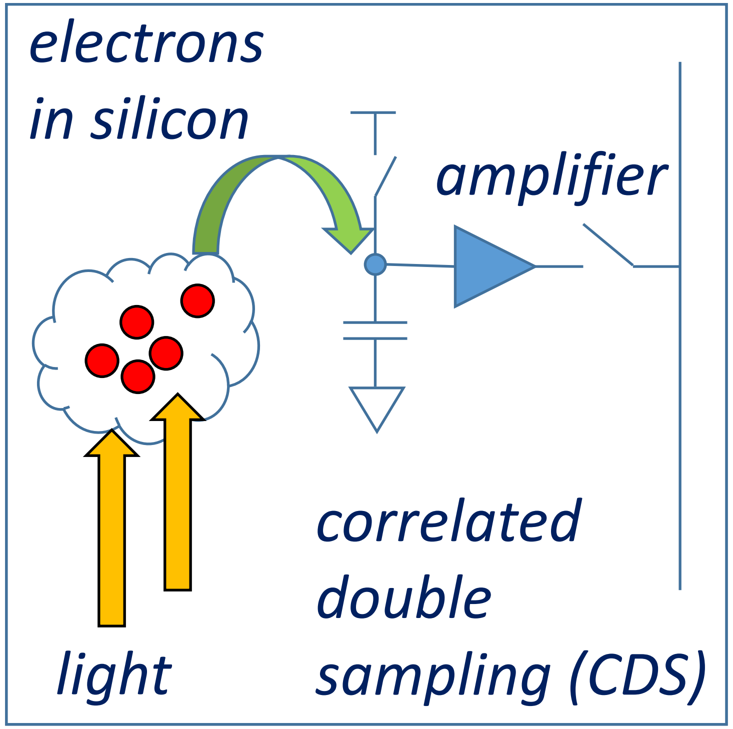


Fig. 10. JPL CMOS-compatible lateral APS.

Well understood and accepted in 2025. Not so much in 1993.

CMOS image sensor: Combine best features of 3T-APS and CCDs

Intra-pixel Charge Transfer Enables Low Readout Noise

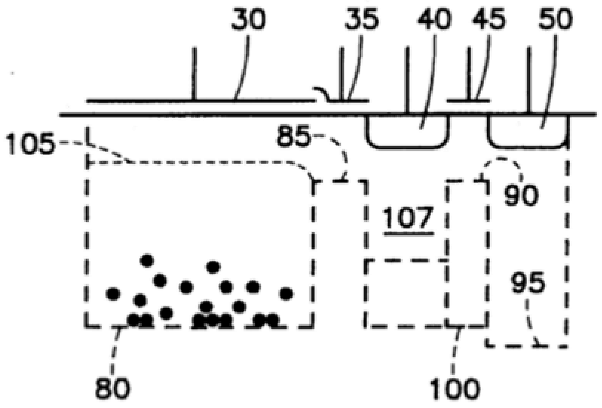


Floating diffusion amplifier
Walter Kosonocky, 1970s

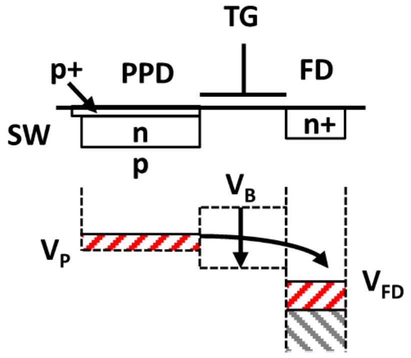
Correlated double sampling
Marvin White, 1973

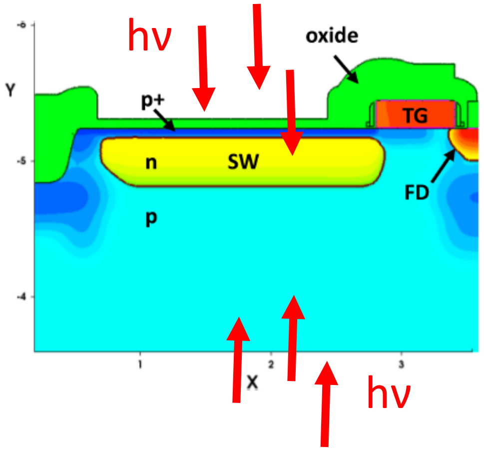
Pinned photodiode
Nobukazu Teranishi, 1982

Double-poly process (JPL 1993)



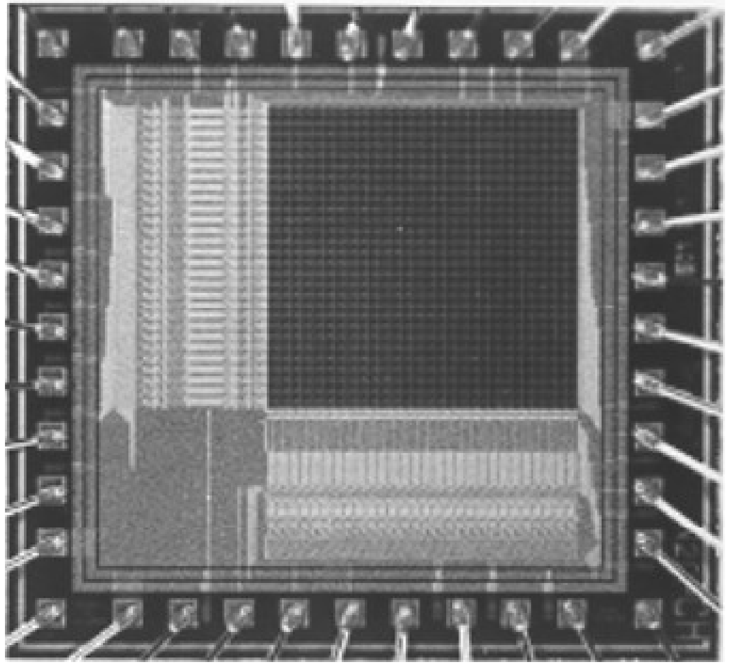
Low voltage pinned photodiode process (25V → 5V
(Kodak+JPL 1995)





First CMOS image sensor with intra-pixel charge transfer. Worked the first time! JPL/Caltech April 1993

Jet Propulsion Laboratory



Chip (28x28 pixels)

"George"

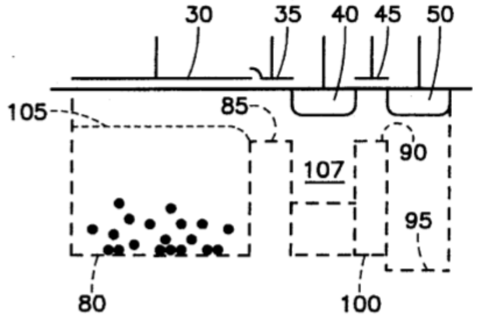
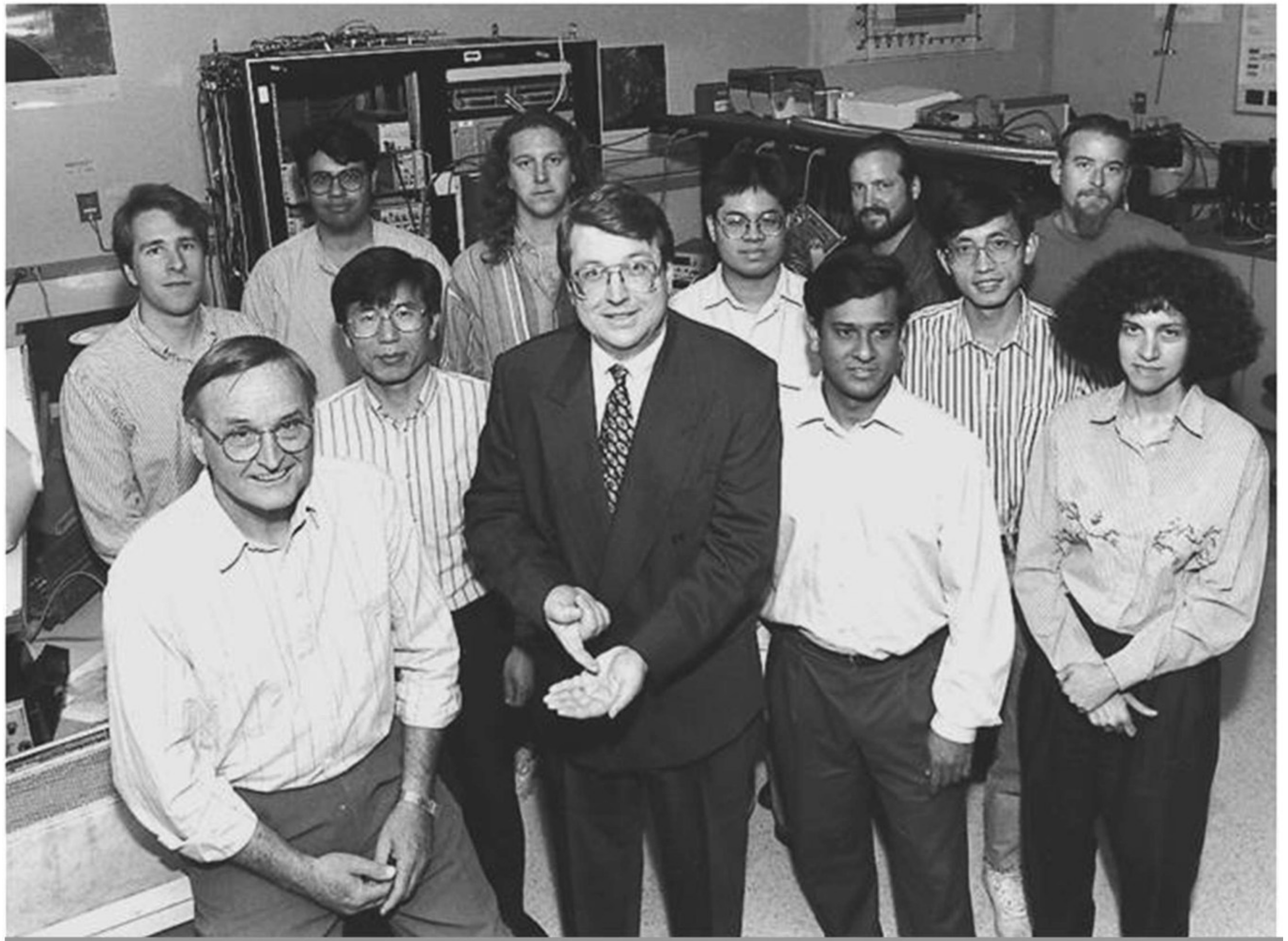


FIG. 4

CMOS active pixel sensor with intra-pixel charge transfer
US Patent 5,471,515 Fossum, Mendis, Kemeny

Jet Propulsion Laboratory

JPL team 1995



Advanced Imager Technology Group, Jet Propulsion Laboratory, California Institute of Technology 1995
Back row: Roger Panicacci, Barmak Mansoorian, Craig Staller, Russell Gee, Peter Jones, John Koehler
Front row: Robert Nixon, Quisup Kim, Eric Fossum, Bedabrata Pain, Zhimin Zhou, Orly Yadid-Pecht

Not pictured: Prior members Suni Mendis, Sabrina Kemeny, Junichi Nakamura

Accidental discovery/ invention by our collaborators at AT&T Bell Labs 1994

ISSCC95 / SESSION 13 / IMAGE SENSORS AND SYSTEMS / PAPER TP 13.5

TP 13.5: A 256x256 CMOS Active Pixel Image Sensor with Motion Detection

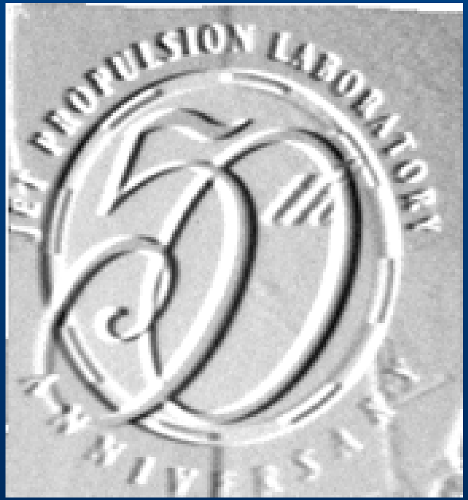
Alex Dickinson, Bryan Ackland, El-Sayed Eid,
David Inglis, Eric R. Fossum*

AT&T Bell Laboratories, Holmdel, NJ
*Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA

MOTION DETECTION

Motion to left

Normal image



Motion to right

- Use floating diffusion as analog frame memory
- No change to pixel design, just timing

Jet Propulsion Laboratory

Luck is often an element of an entrepreneur's tale

Biz
Week
March
1995

NASA'S TINY CAMERA HAS A WIDE-ANGLE FUTURE

It may still be in the lab, but the latest advance in capturing images has very bright prospects, indeed

Get ready for the camera-on-a-chip. Since the 1970s, camera makers have dreamed of a one-chip camera containing all the components necessary to take a snapshot or make a movie. With all the smarts on one chip instead of several, designers figure they could make a camera small and cheap enough to open vast new markets for everything from dolls that "see" to rear-bumper cameras that would help drivers back up.

Such devices are impractical with today's standard electronic image sensor. It's called a CCD, for charge-coupled device, and it's at the heart of every fax machine and camcorder. Japanese powerhouses such as Sony, Matsushita, and NEC churn out millions a year. CCDs offer good image quality. But they are costly, power-hungry, and—with the accessory chips they require—bulky.

TEAMWORK. Now, the one-chip dream

1994 JPL
Mockup
vs.
2025
Apple 17 Pro
3 cameras

~same scale

Technology Transfer

Entrenched industry moves slowly in adopting new technologies so in February 1995 we founded **Photobit Corporation** to commercialize the CMOS image sensor technology ourselves

S.Kemeny, N. Doudoumopoulos, E. Fossum, R. Nixon
(later R. Panicacci 1st employee/5th co-founder)

INTERNATIONAL IMAGE SENSOR SOCIETY

1997 IEEE Workshop on

Charge-Coupled Devices and Advanced Image Sensors

June 5-7, 1997

Holiday Inn Crowne Plaza

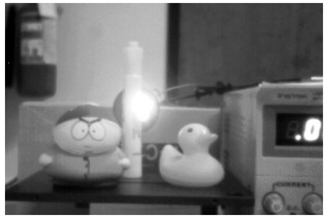
Bruges, Belgium

Perspiration phase

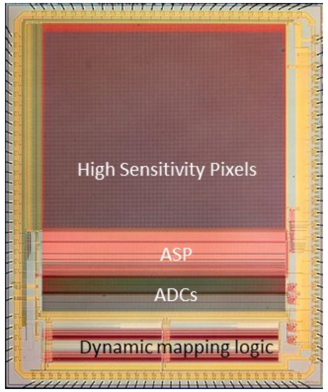
1995-2001 Photobit grows to about 135 persons

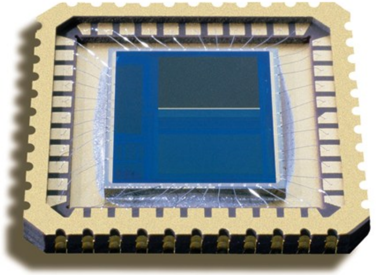
- Self-funded with custom-design contracts from private industry
- Important support from SBIR programs (NASA/DoD)
- Later, investment from strategic business
- Over 100 new patent applications filed

November 2001 Photobit acquired by Micron Technology



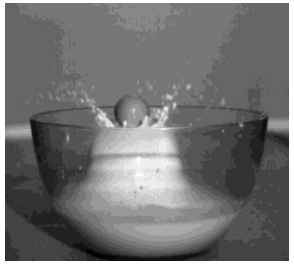
>100dB HDR for Automotive





Webcams (Intel, Logitech)

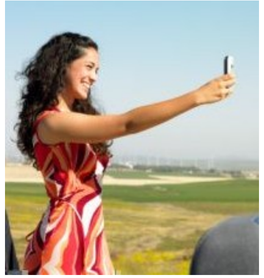
1st Pill Camera (Given Imaging)



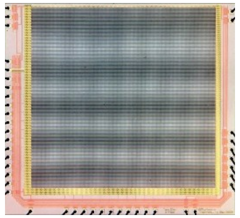
1st 500-1000fps Mpix+ global shutter for high speed motion capture and machine vision

1st Light, Auto high beams, & Rain sensor (Gentex)

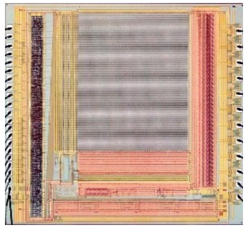
"Killer"app



1st CMOS Dental X-ray Sensors



30+Mrad-hard Star Tracker

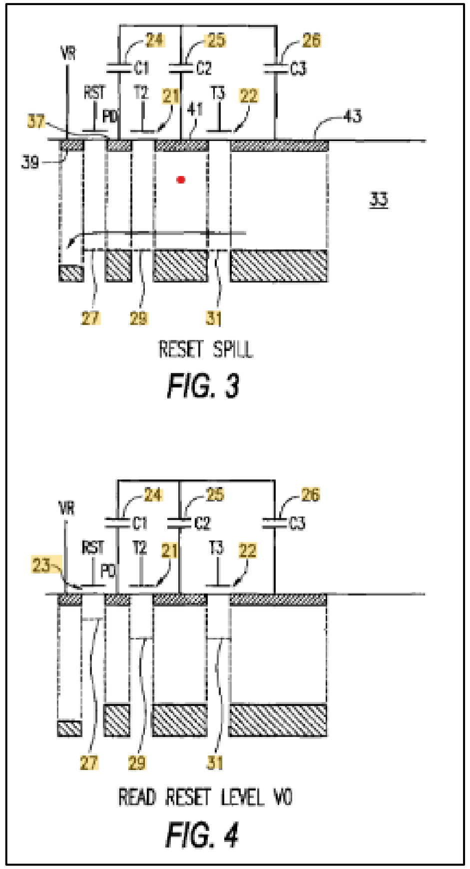


Photobit Corporation team
(early 2000)

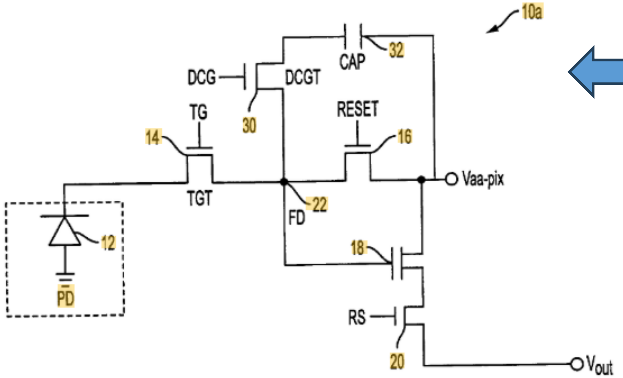
Missing: Oslo Design Center, Tokyo Design Center

Micron HDR – Cascaded Integration

FOSSUM US 6,888,122 and US 7,990,449 priority date Aug. 29, 2002 (expired) High dynamic range cascaded integration pixel cell and method of operation. Reduced to practice at Micron Imaging Japan Office (Junichi Nakamura, Isao Takayanagi for 3T operation)

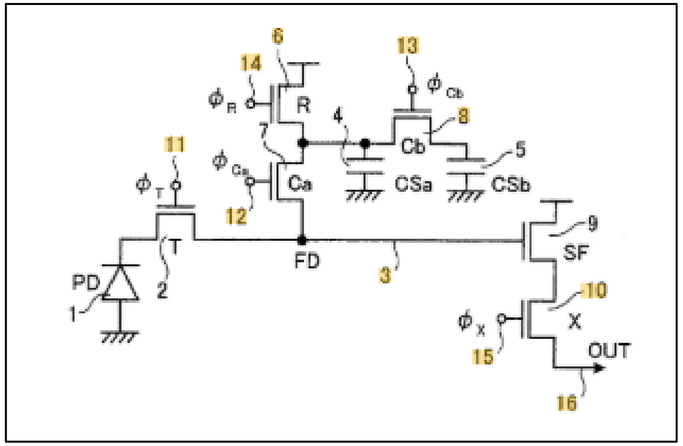


RHODES and HONG US 7,075,049 priority date June 11, 2003 (expired) Dual conversion gain imagers. 121 claims



SUGAWARA and AKAHANE JP 5,066704 priority date April 7, 2005 (expired?) Solid-state imaging device and method of operating solid-state imaging device aka “LOFIC”

Tohoku Univ - nearly identical to cascaded integration concept but added 4T operation. Cites 6,888,122



At 30 years the technology has an adult life of its own

DARTMOUTH

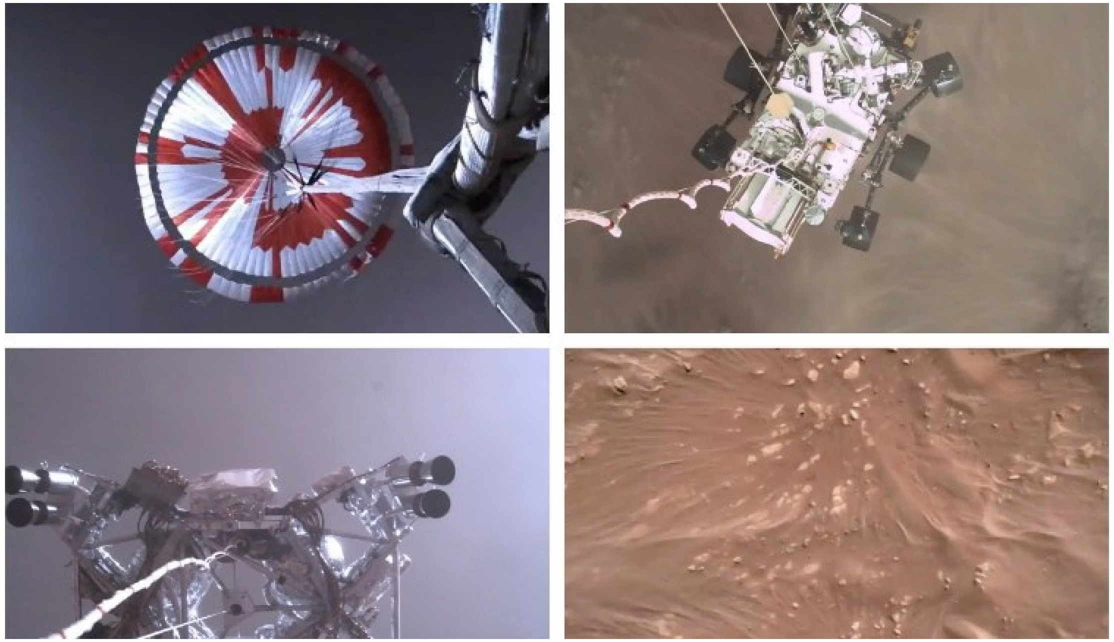
- Thousands of engineers working on this around the globe.
- Caltech licensed its patents to all the major players.
- Today, about 6-7 billion cameras are manufactured each year that use the CMOS image sensor technology we invented at JPL, or about 200 cameras per second.
- Semiconductor sales of CMOS image sensors is about $30B/yr.
- NASA has finally adopted the technology for use in space.

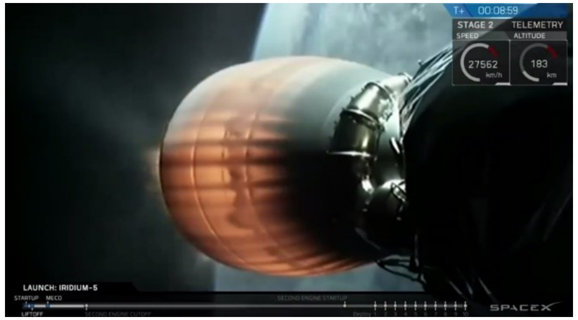
NASA'S TINY CAMERA HAS A WIDE-ANGLE FUTURE

It may still be in the lab, but the latest advance in capturing images has very bright prospects, indeed

Promise Fulfilled for Space Applications!

Mars Perseverance landing 02/2021 (~20 CMOS cameras on board!)





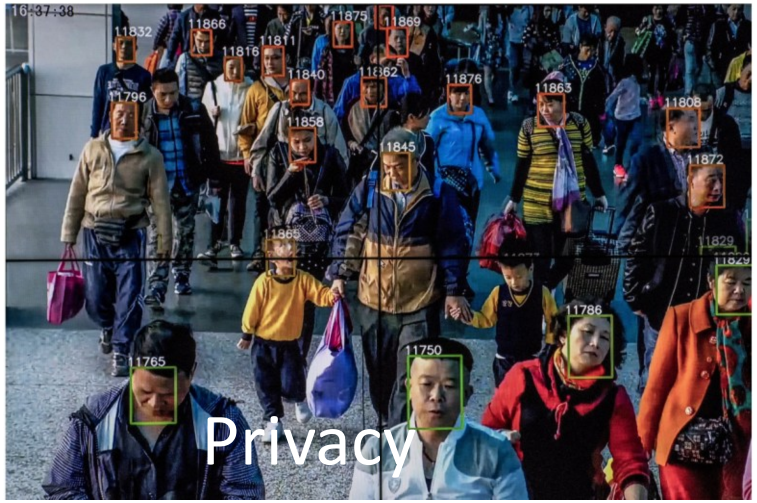
SpaceX Falcon 9 - 3/30/2018

DART asteroid impact mission 9/26/2022

Image from Italian Space Agency's LICIACube Satellite

DARTMOUTH

New technology invariably brings new social issues



vs.

Facebook Instagram zoom YouTube TikTok

Small eyes and bombs

in the sky

2017 Queen Elizabeth Prize for Engineering

DARTMOUTH

Eric Fossum | Nobukazu Teranishi | Mike Tompsett

CMOS image sensor | Pinned photodiode | CCD image sensor

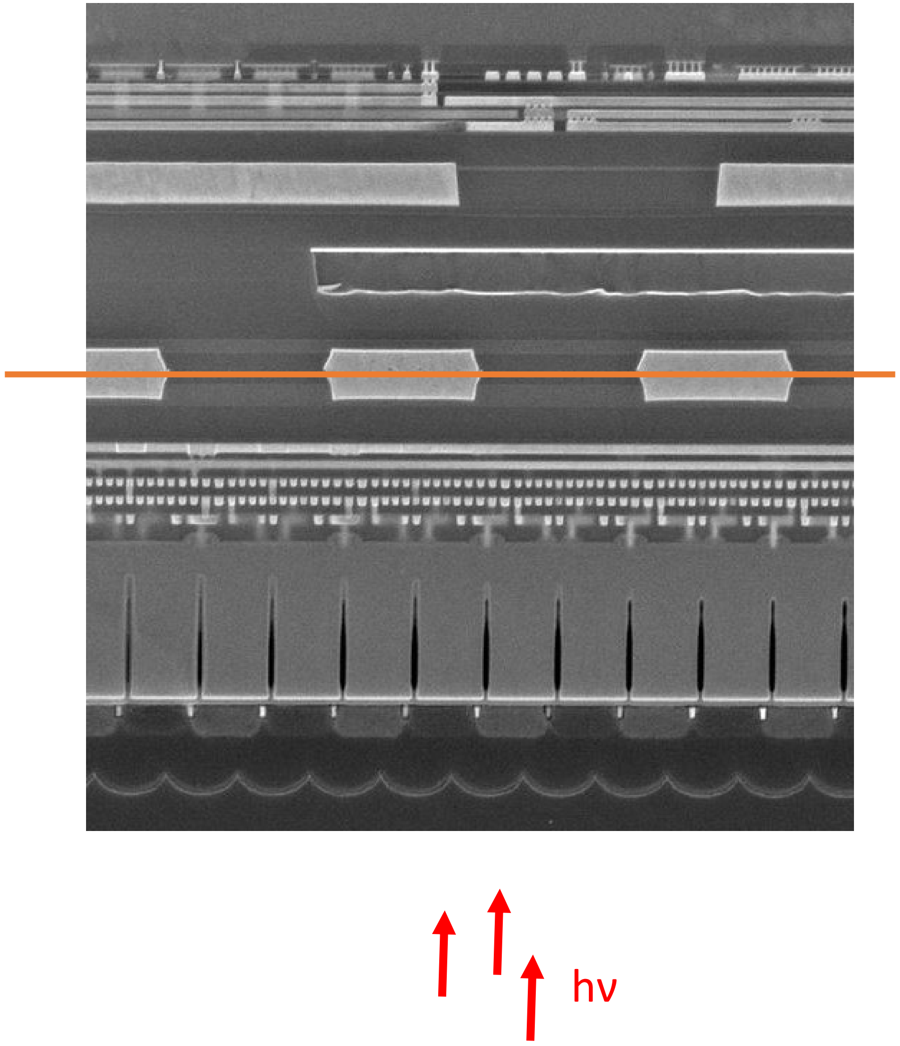
+ George Smith CCD

For the creation of digital imaging sensors

HRH Prince Charles
Buckingham Palace Reception
December 2017

Some More Recent Advancements in CMOS Image Sensors

1. 3D stacking technology
2. Metalenses and color routing
3. Spectral extension, quantum dots
4. Ranging sensors (dToF, iToF)
5. Edge/smart sensors
6. DVS image sensors
7. Global shutter
8. High dynamic range
9. >100Mpixels, ~0.5um pixel sizes
10. Photon-counting image sensors



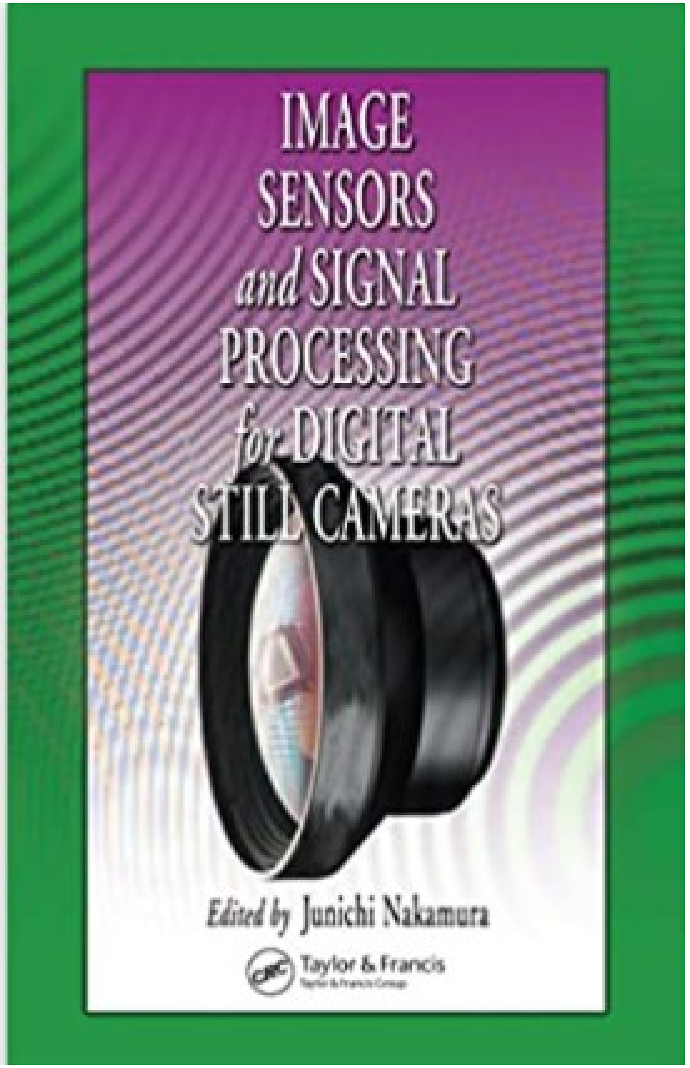
DARTMOUTH

Quanta Image Sensors (QIS)

CMOS image sensor type (CIS-QIS)
&
SPAD type (SPAD-QIS)

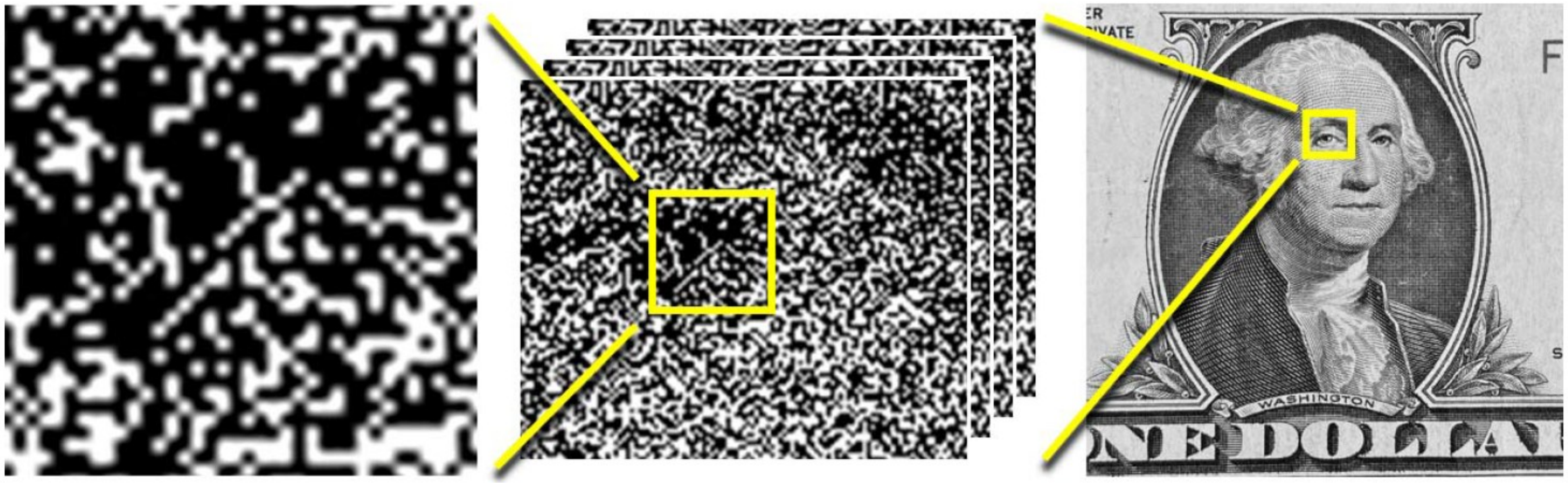
Quanta Image Sensor Origin Story

- Around 2003-2004 Junichi Nakamura was preparing his book.
- Asked me to write the last chapter on “the future of image sensors”
- Extrapolated to a future of a billion pixels with submicron pitch and full-well capacity of just 1e-.

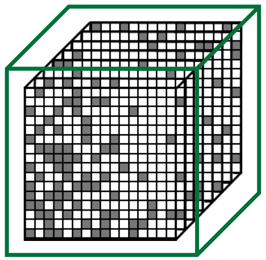


DARTMOUTH

Quanta Image Sensor (QIS)
"Count Every Photon"



Computational image reconstruction
X-Y-t Bit Density ➔ Gray Scale



Cubicle

Specialized pixel ➔ "jot"

Vision: A billion pixels readout at 1000 fps (1Tb/s) with single photon-counting capability and consuming less than a watt.

US Patent 9,225,918 Priority May 27, 2005

DARTMOUTH

Imaging Paradigm Shift

- Might seem like a lot of extra work compared to an integrating bucket of charge in conventional CMOS image sensors (CIS).
- Counting every (visible) photon is about as sensitive as one can get for photography, security, defense, space, etc.
- Helps with small pixel vs. full-well capacity trade off.
- Allows new capabilities in computational imaging such as:
  - Trade off in sensitivity and resolution that can be scene-dependent or attention-dependent.
  - Permits time-delay and integration in multiple independent tracks and arbitrary directions.
  - Allows motion blur compensation for multiple targets.
  - Allows high apparent SNR for very low photon flux.
- Reinvented/Rebranded ~2020 by CS folks as "Quanta Burst Photography"

E.R. Fossum, The Quanta Image Sensor (QIS): Concepts and Challenges (invited) in Proc. 2011 Opt. Soc. Am. Topical Meeting on Computational Optical Sensing and Imaging, Toronto, Canada July 10-14, 2011. https://opg.optica.org/abstract.cfm?URI=COSI-2011-JTuE1

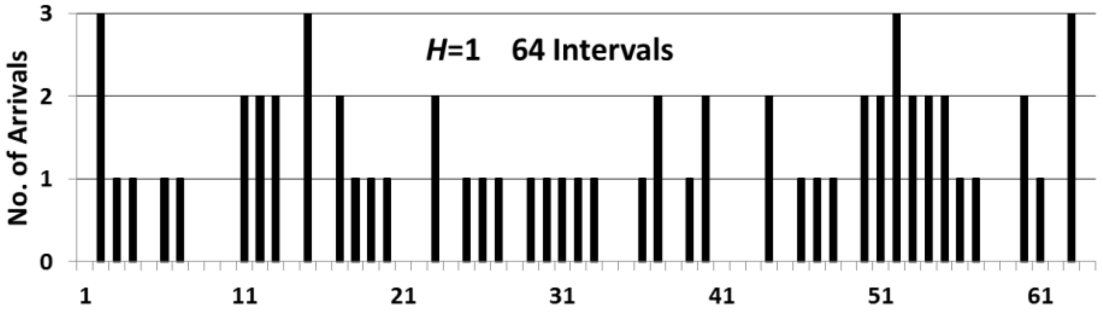
Photon and photoelectron arrival rate described by Poisson process

Define *quanta exposure* $H = \phi\,\tau$ $\quad$ $H = 1$ means expect 1 arrival on average.

Probability of k arrivals

$$P[k] = \frac{e^{-H}\,H^{k}}{k!}$$

Monte Carlo



For 1b QIS, only two states of interest

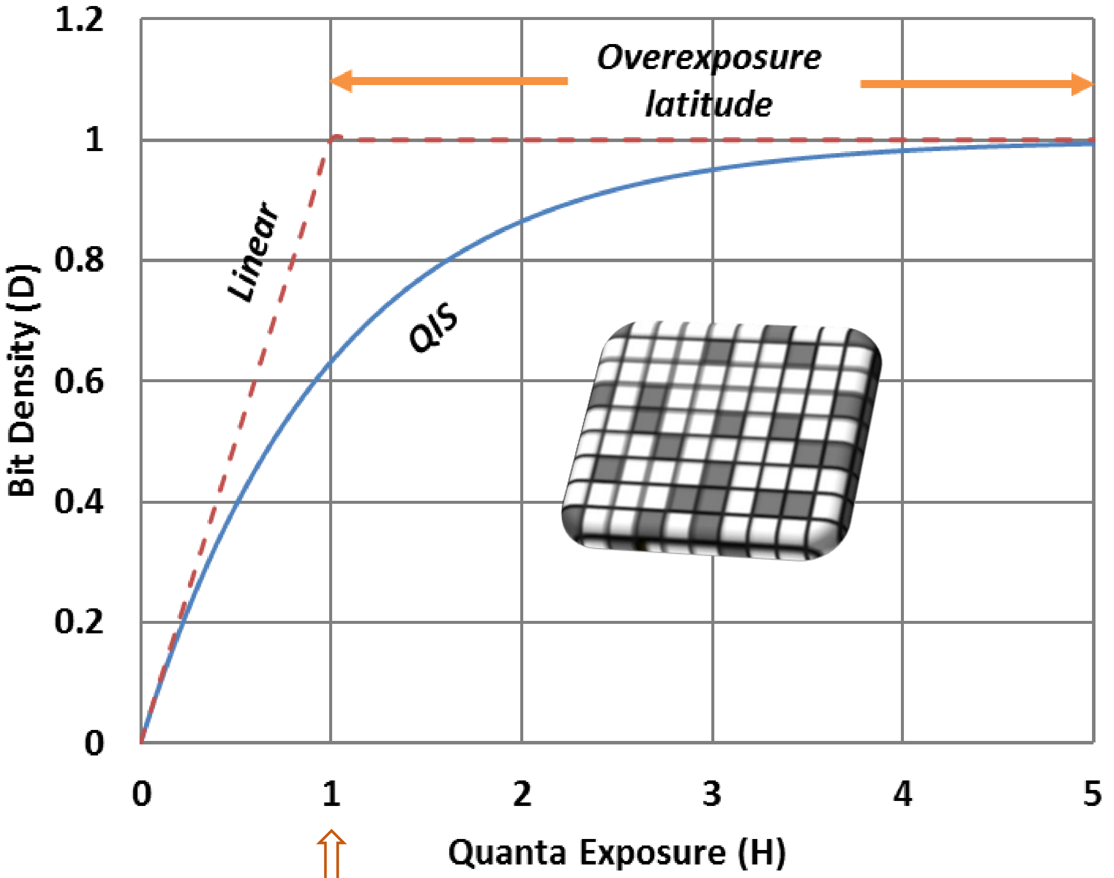
$$P[0] = e^{-H}$$

$$P[k>0] = 1 - P[0] = 1 - e^{-H}$$

For ensemble of *M* jots, the expected number of 1's : $M_1 = M \cdot P[k>0]$

Photoresponse as bit density

$$Bit\ Density\ D \triangleq \frac{M_1}{M} = 1 - e^{-H}$$

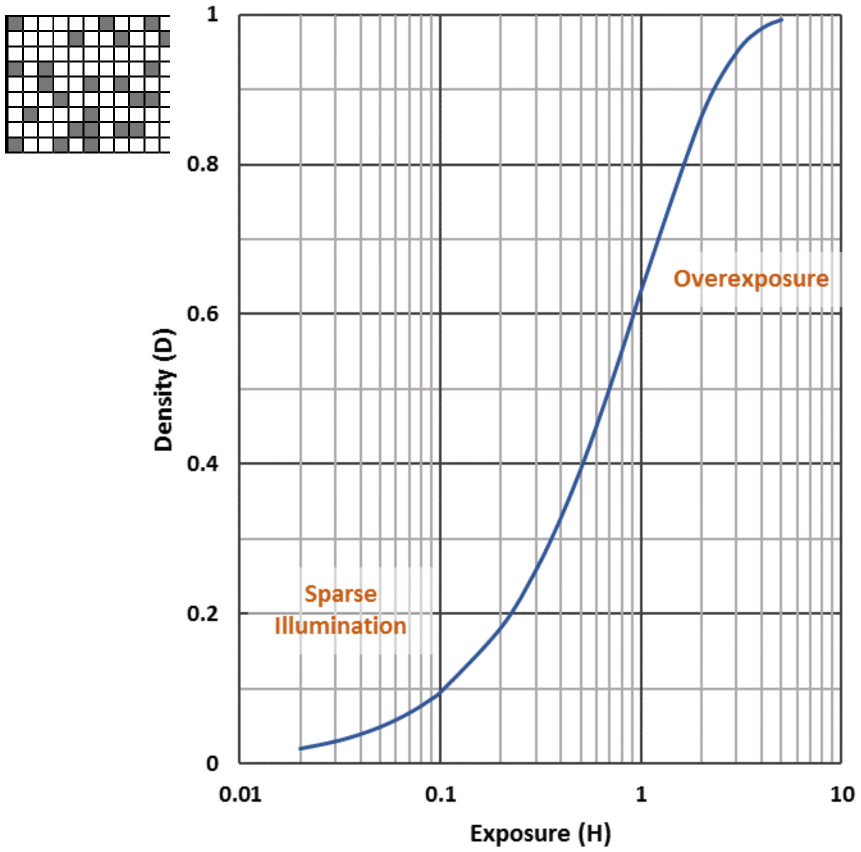


Average of one arrival per jot per integration time

QIS responds to light like film

$$Bit\ Density\ D \triangleq \frac{M_1}{M} = 1 - e^{-H}$$

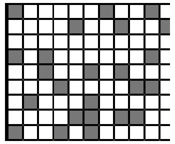
QIS D – log H

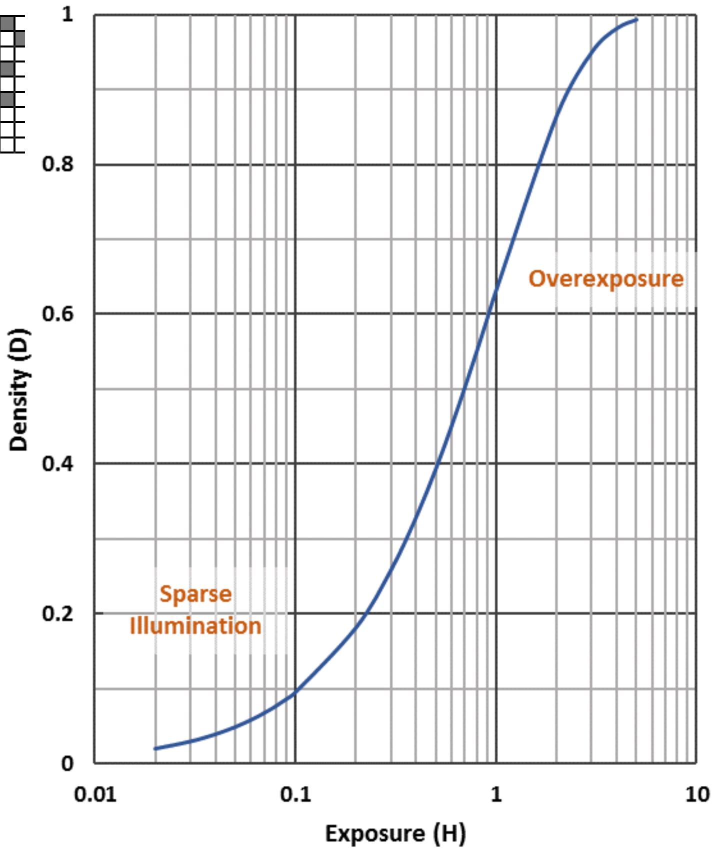


Bit Density vs. Exposure

QIS responds to light like film

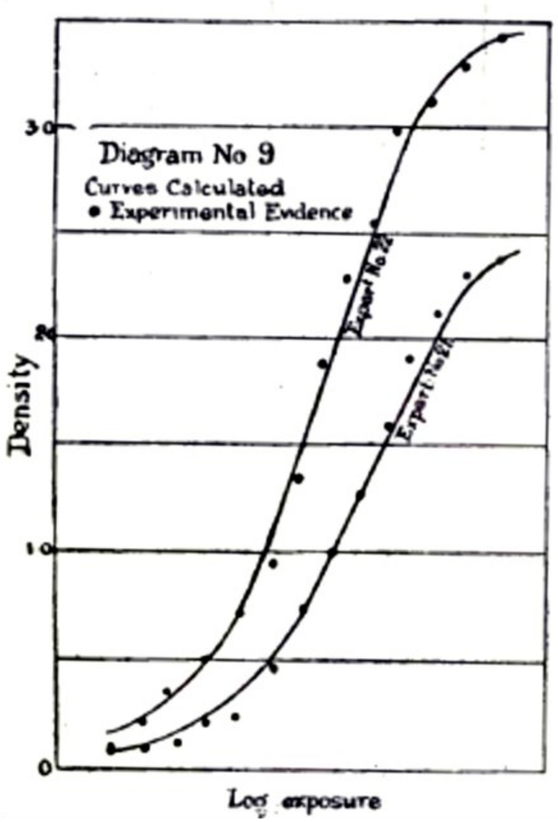
QIS D – log H



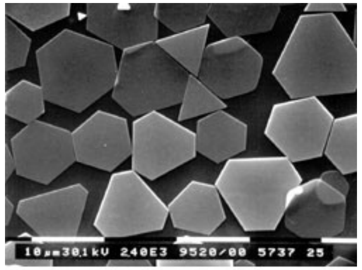


Bit Density vs. Exposure

Film D – log H



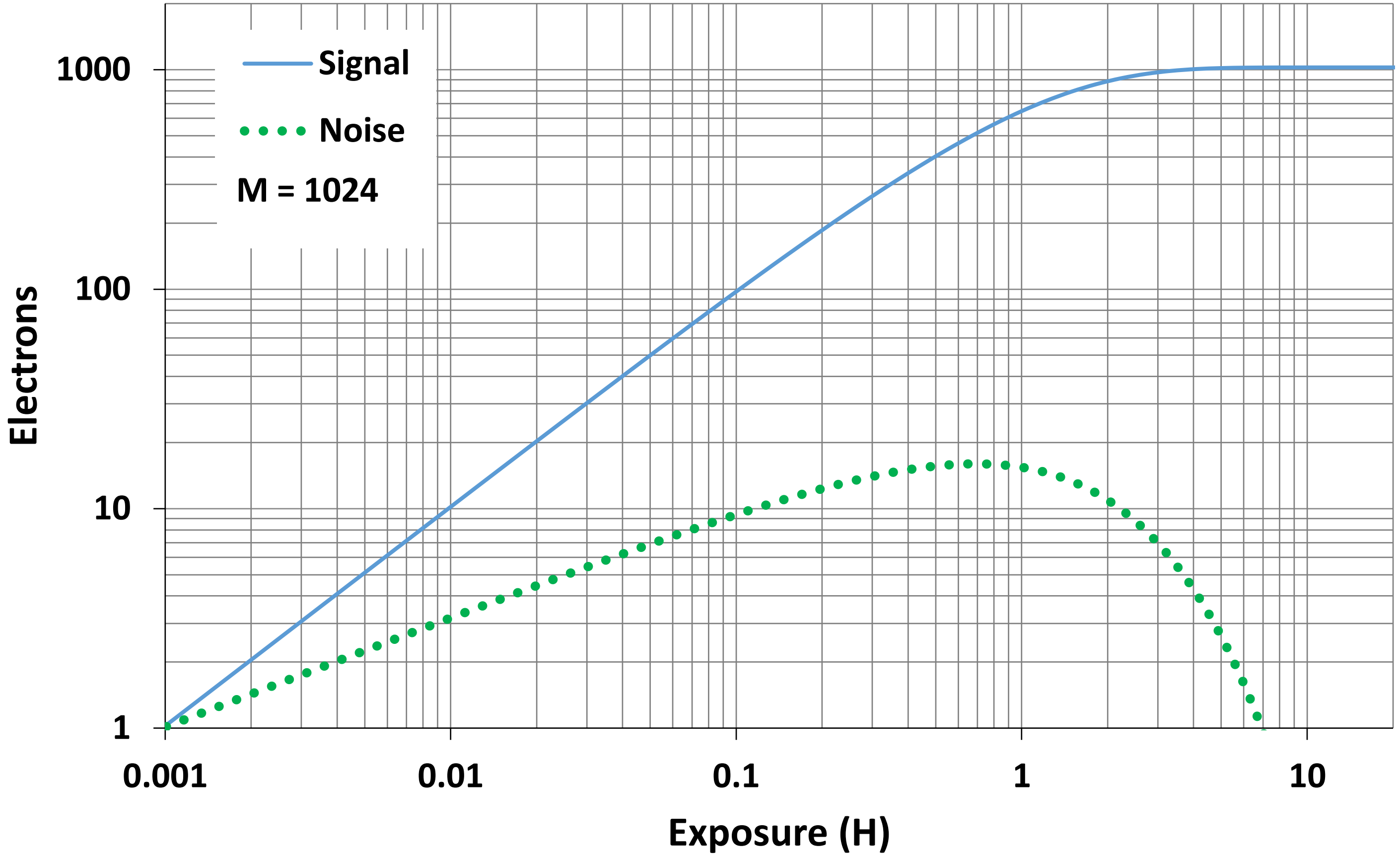
Film Density vs. Exposure
1890 Hurter and Driffield



Electron micrograph of tabular grain emulsion

http://faculty.virginia.edu/ASTR5110/lectures/detectors/detectors_intro.html

Signal and Noise Model for QIS

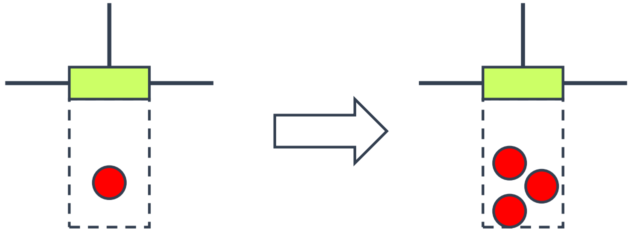


Fossum, IEEE JEDS vol 1(9) pp. 166-173 Sept 2013

Multi-bit jot increases flux capacity

At the flux capacity, there is an average of $2^n - 1$ photoelectrons per *n*-bit jot

$$\phi_{wn} = jf_r(2^n - 1)/\delta\bar{\gamma}$$



Single bit jot
0, 1 electrons

Multi-bit (2b) jot
0, 1, 2, 3 electrons

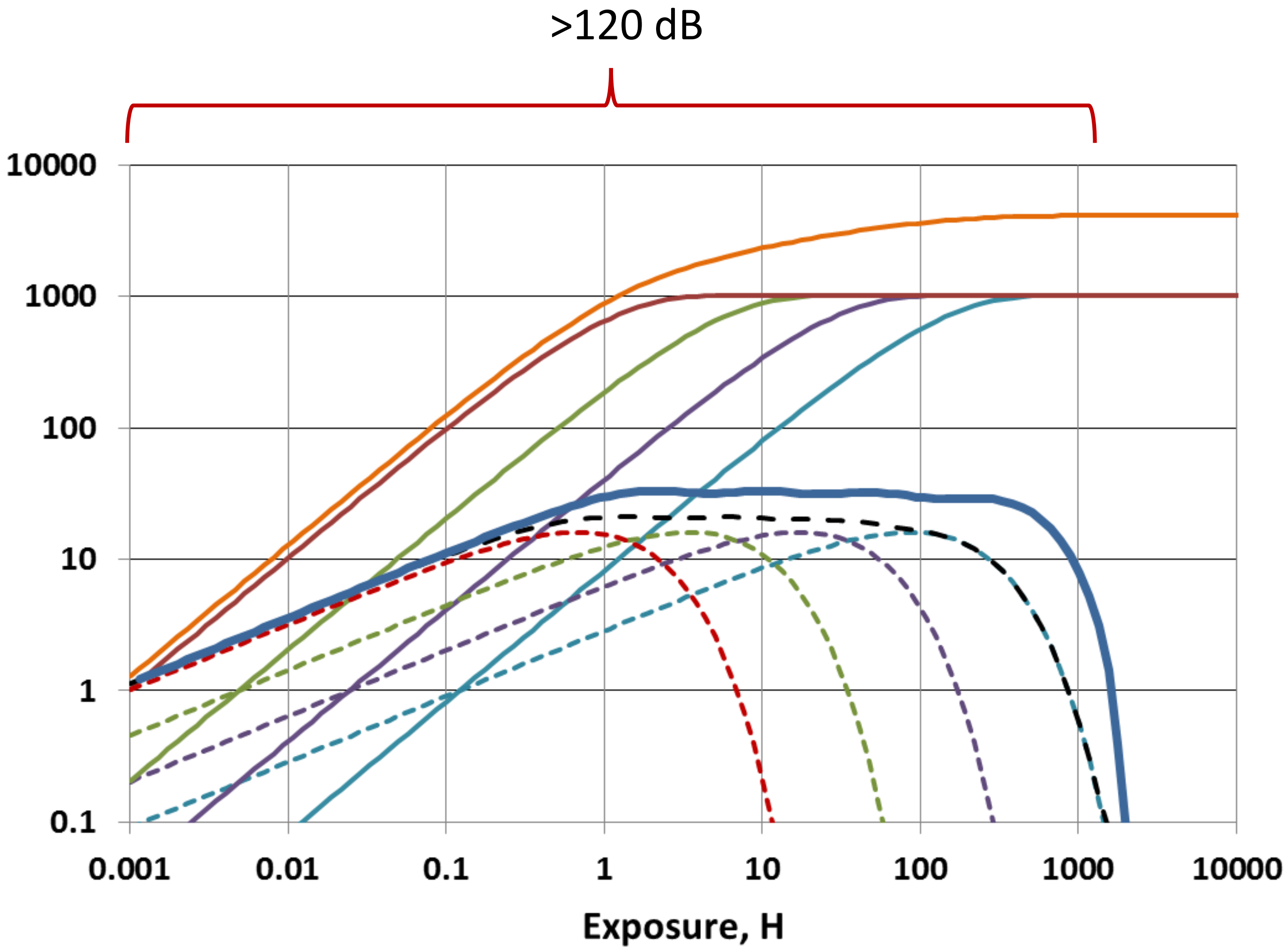
➔ Can increase flux capacity at same jot density and field readout rate
➔ Or, relax field readout rate and/or jot density for same flux capacity

Little impact on detector and storage well. Little impact on FD CG or voltage swing (e.g. 1mV/e -> 31mV swing for 5b jot.

High Dynamic Range with 1b QIS

16x16x16 cubicle

Sum of 16 fields
4@ δ =1.0
4@ δ =0.2
4@ δ =0.04
4@ δ =0.008



Fossum, IEEE JEDS vol 1(9) pp. 166-173 Sept 2013

Initial Issues with SPADs for 1bQIS application

DARTMOUTH

<u>SPADs use avalanche multiplication for gain</u>

- High internal electric fields
- Higher operating voltages (15-20V)
- Larger pixels (8-25um)
- High dark count rates (100-1000Hz)
- Dead time
- Low fill factor (low PDE <50%)
- Low manufacturing yield
- Small array sizes (below 0.1M jots)
- Do not resolve photon number
- “Big” energy to detect single photon event

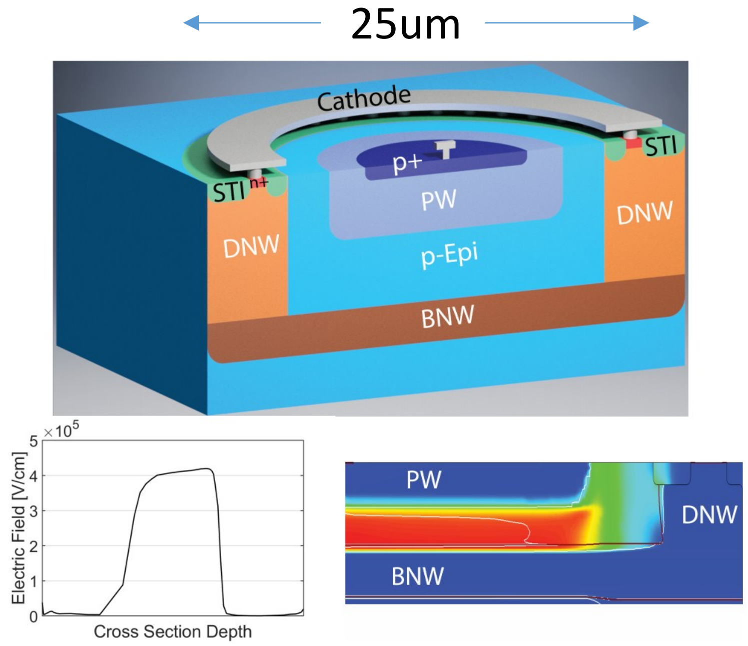


Fig. 2. SPAD cross-section (*top*) and TCAD simulation of the electric field (*bottom*). A quantification of the electric field along the vertical axis is also shown (*left-side*).

2021 IEEE JSTQE Gramuglia et al

But,

- SPADS have essentially no read noise
- SPADS are excellent for time resolved photon detection
- Things have improved recently for pixel size, DCR and resolution

IEEE TRANSACTIONS ON ELECTRON DEVICES 2015

A SPAD-Based QVGA Image Sensor for Single-Photon Counting and Quanta Imaging

Neale A. W. Dutton, *Member, IEEE*, Istvan Gyongy, Luca Parmesan, Salvatore Gnecchi,
Neil Calder, *Member, IEEE*, Bruce R. Rae, *Member, IEEE*, Sara Pellegrini,
Lindsay A. Grant, *Member, IEEE*, and Robert K. Henderson, *Member, IEEE*

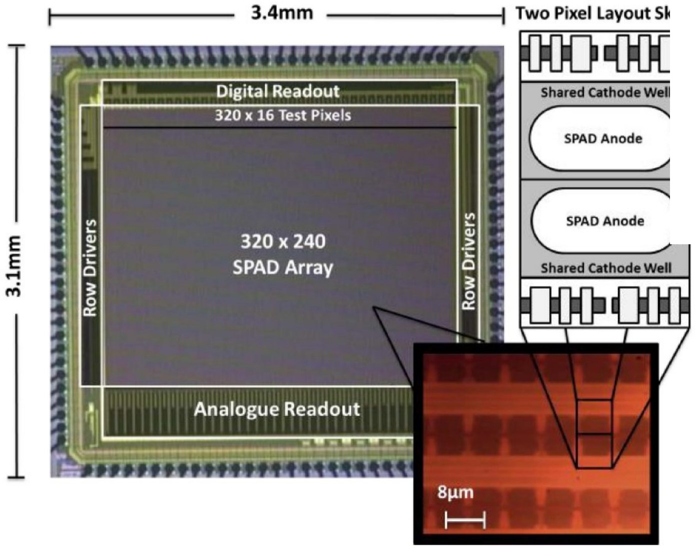
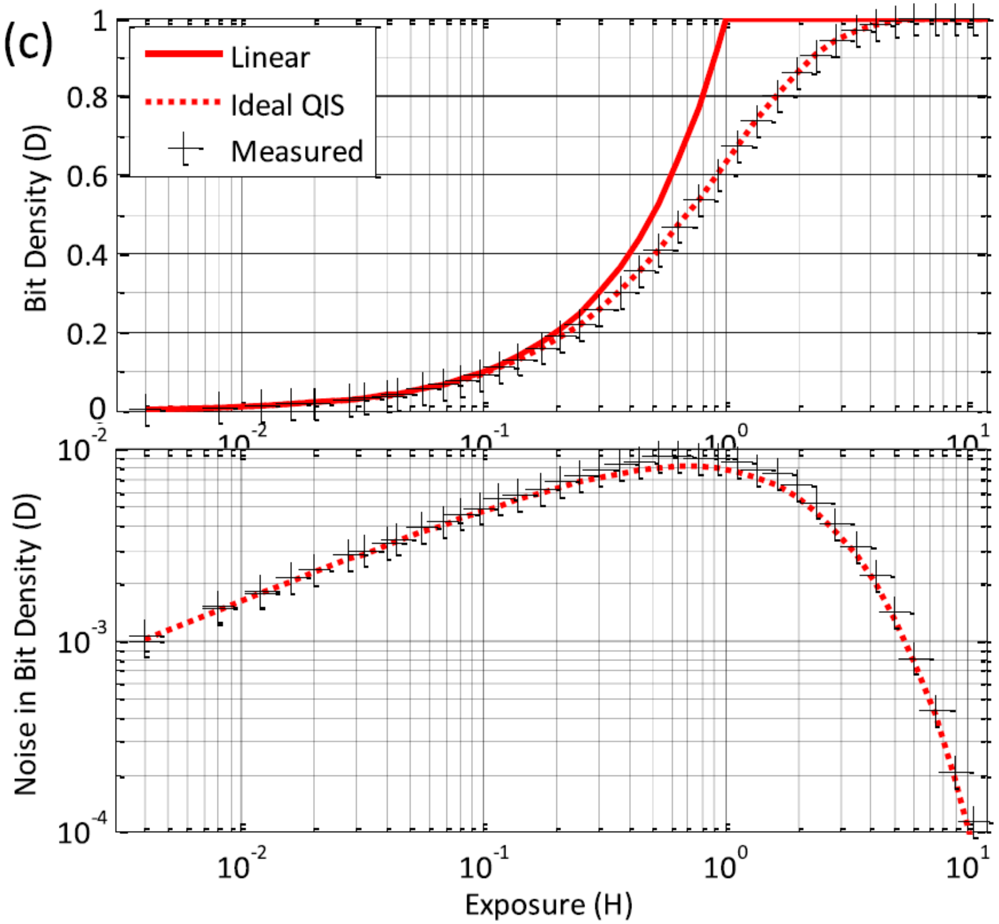


Fig. 1. Photomicrograph of the SPAD-based QVGA imager. Inset: zoomed-in view of the pixel array and layout sketch of the shared-well SPAD structure.



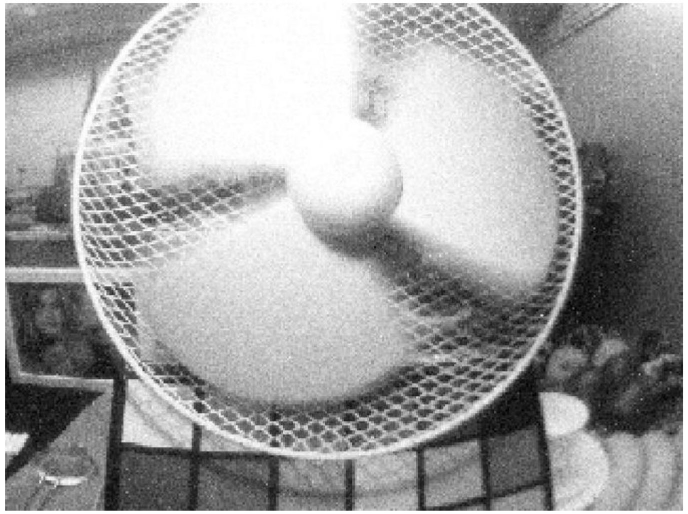


Fig. 6. 5-b QIS frame image consisting of 32 oversampled field images.

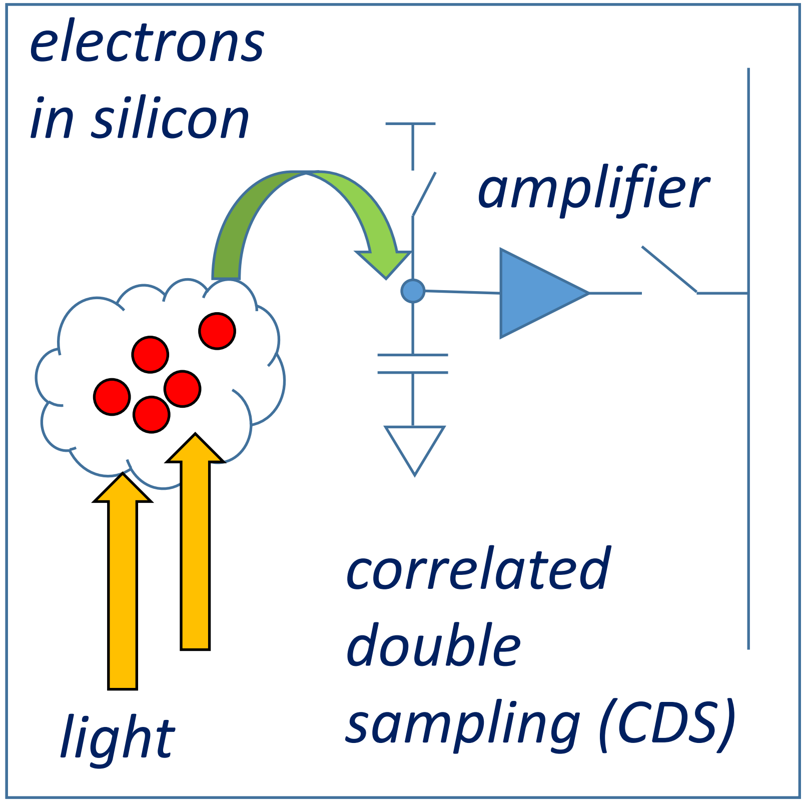
Our approach (CMOS QIS)

No avalanche multiplication, one electron per photon

Use very low capacitance sense node

$\Delta V = \Delta Q / C$

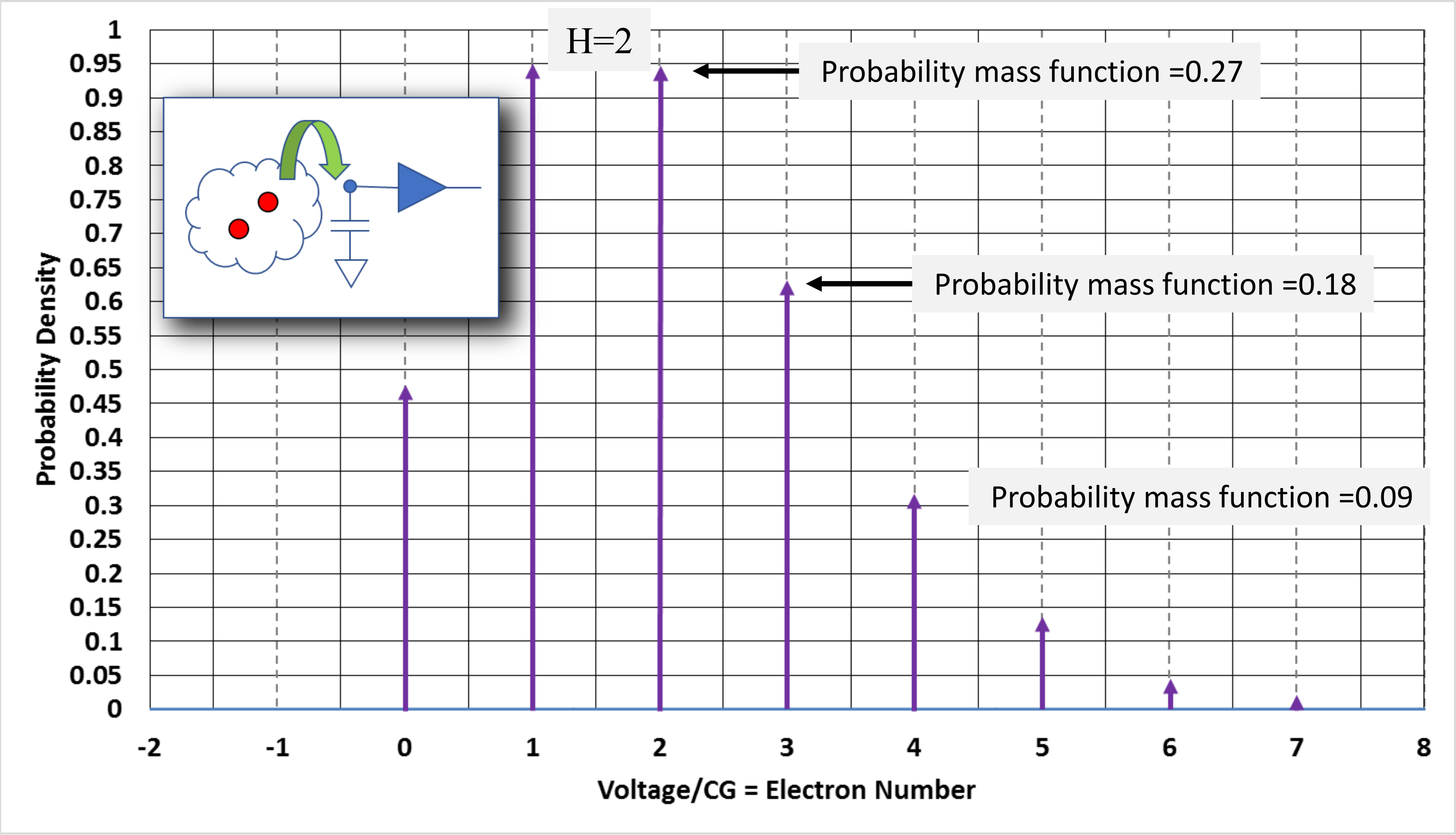
e.g. $1\text{mV} = 1.6\text{x}10^{-19}\text{C} / 160\text{aF}$



Conversion gain CG defined as q/C or volts/electron

Voltage Output with No Electronics Noise

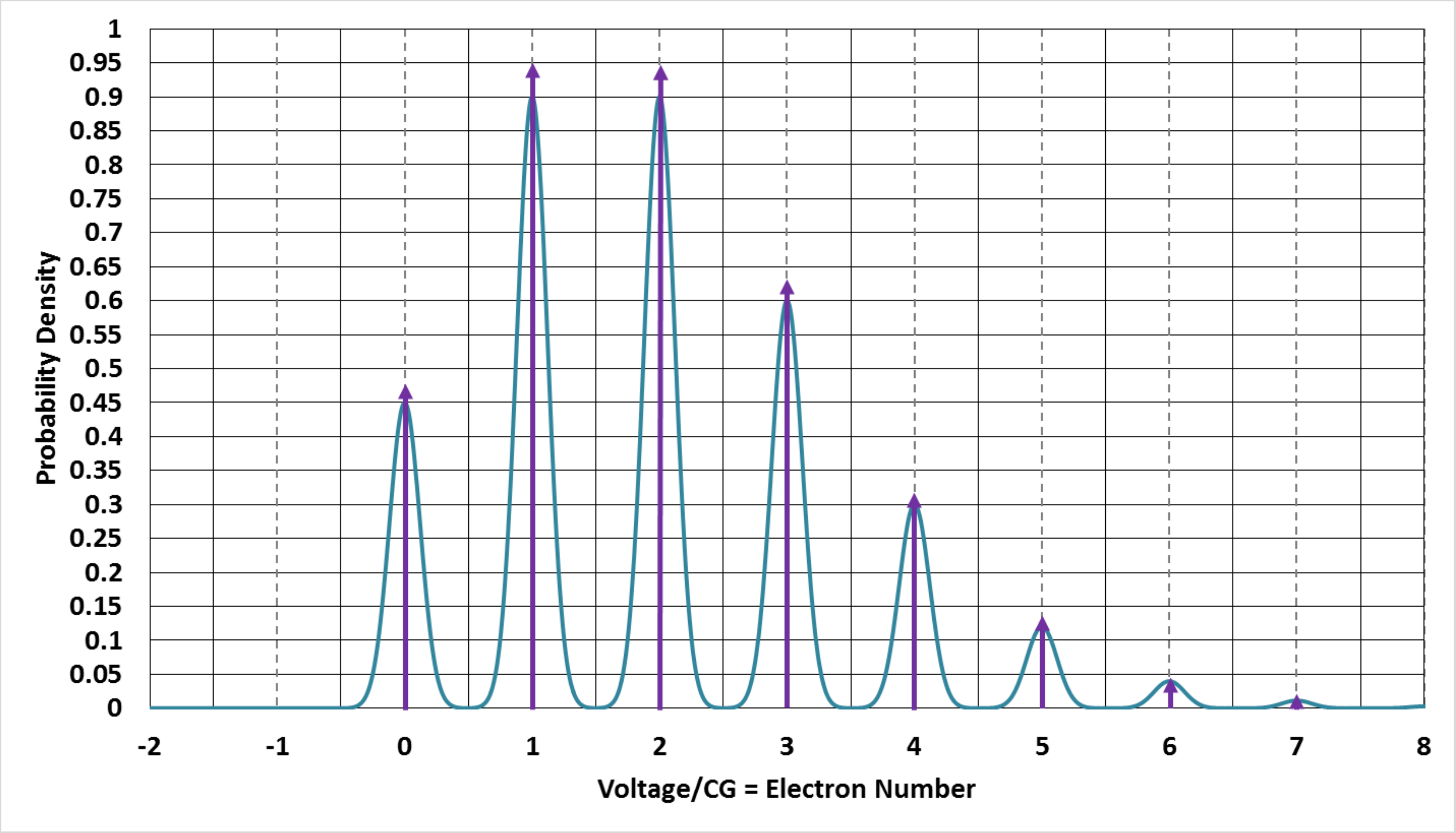
Poisson probability mass function $P[k] = \frac{e^{-H} H^k}{k!}, k = 0, 1, 2, 3 \ldots$



Model

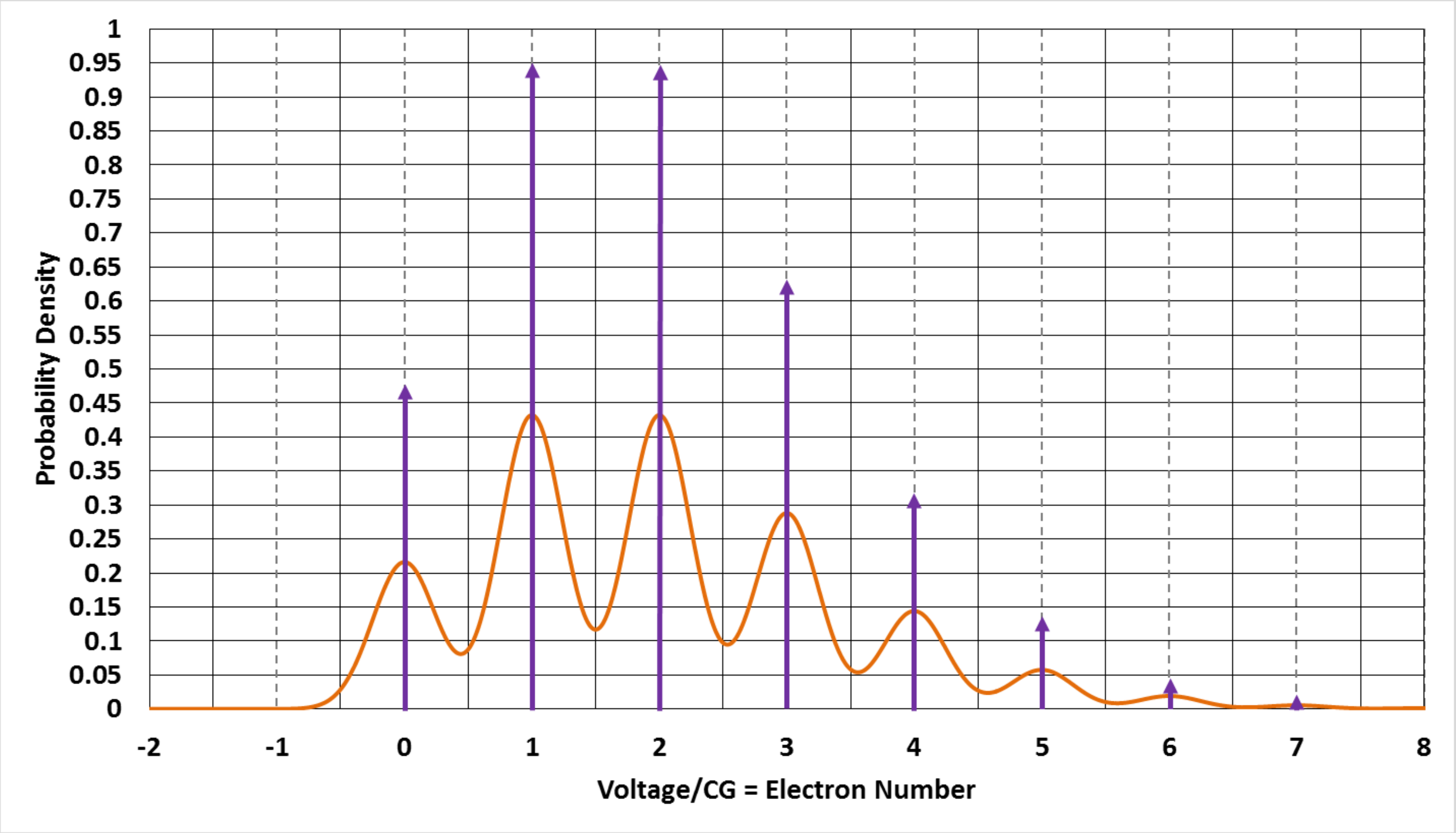
Broadened by 0.12e- rms read noise

$U_n = V_n / CG$ [e- rms]



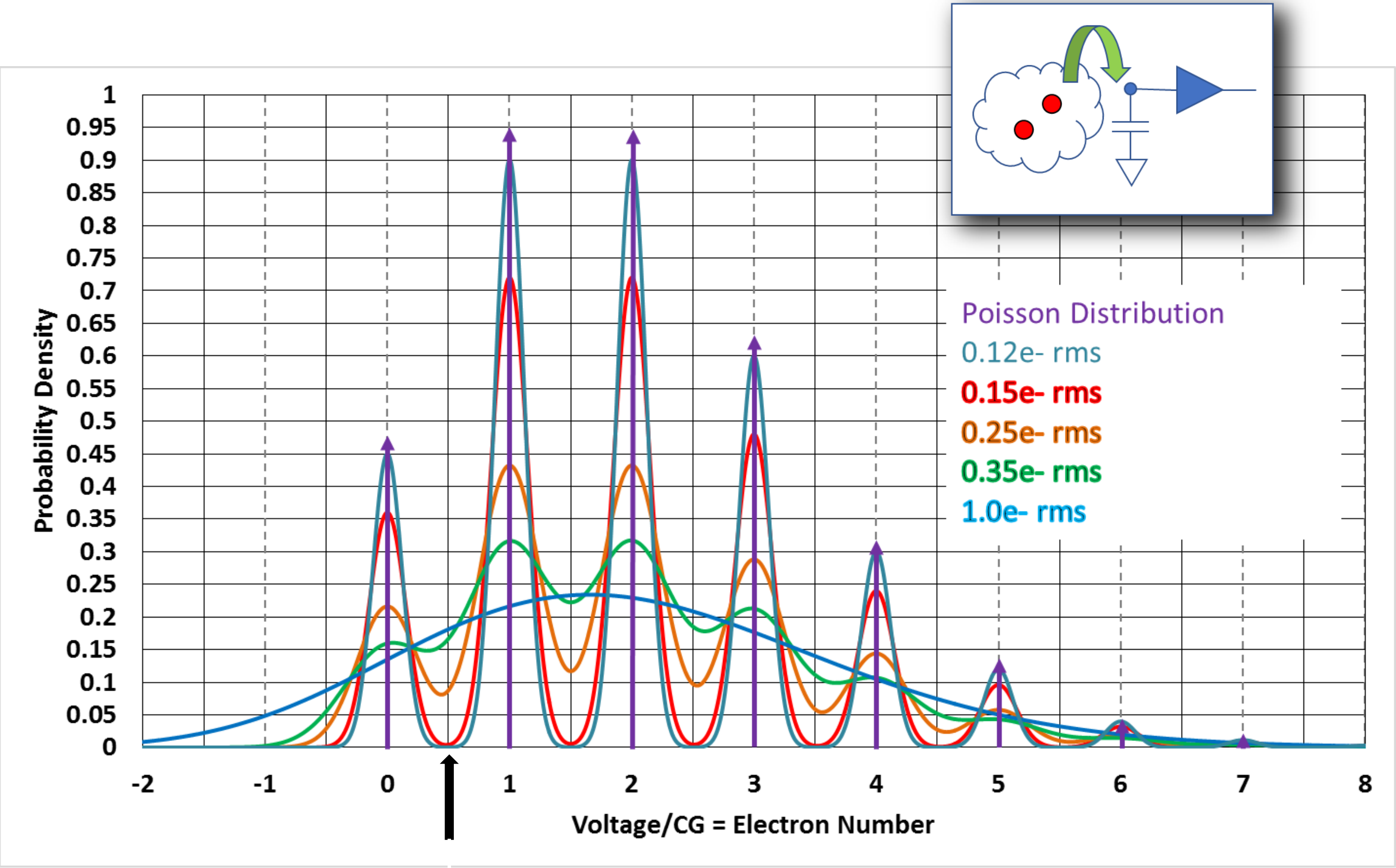
Model

Broadened by 0.25e- rms read noise



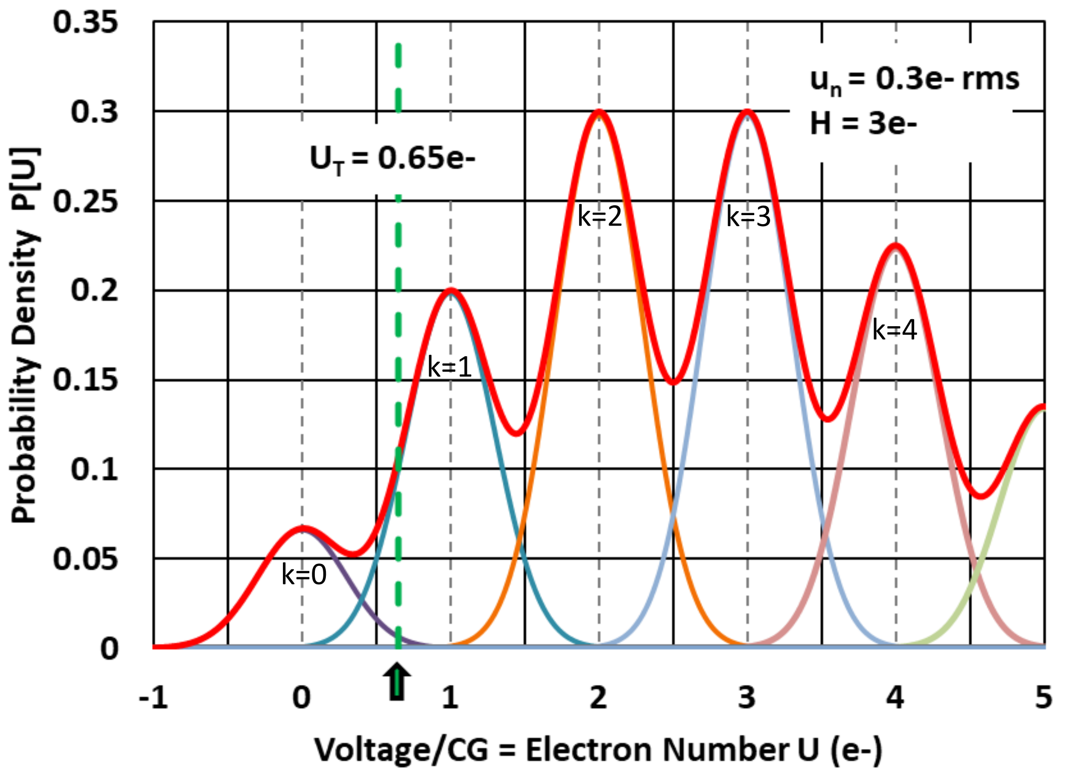
Model

Quantized Values Broadened by Readout Noise



Model

Bit Density Depends on Exposure, Read Noise, and Quantizer



$$D = \frac{1}{2}\sum_{k=0}^{\infty} \mathbb{P}[H + H_{dark}, k]\; erfc\left[\frac{U_T - k}{\sqrt{2}\,u_n}\right] \qquad \mathbb{P}[H,k] = \frac{e^{-H}H^k}{k!}$$

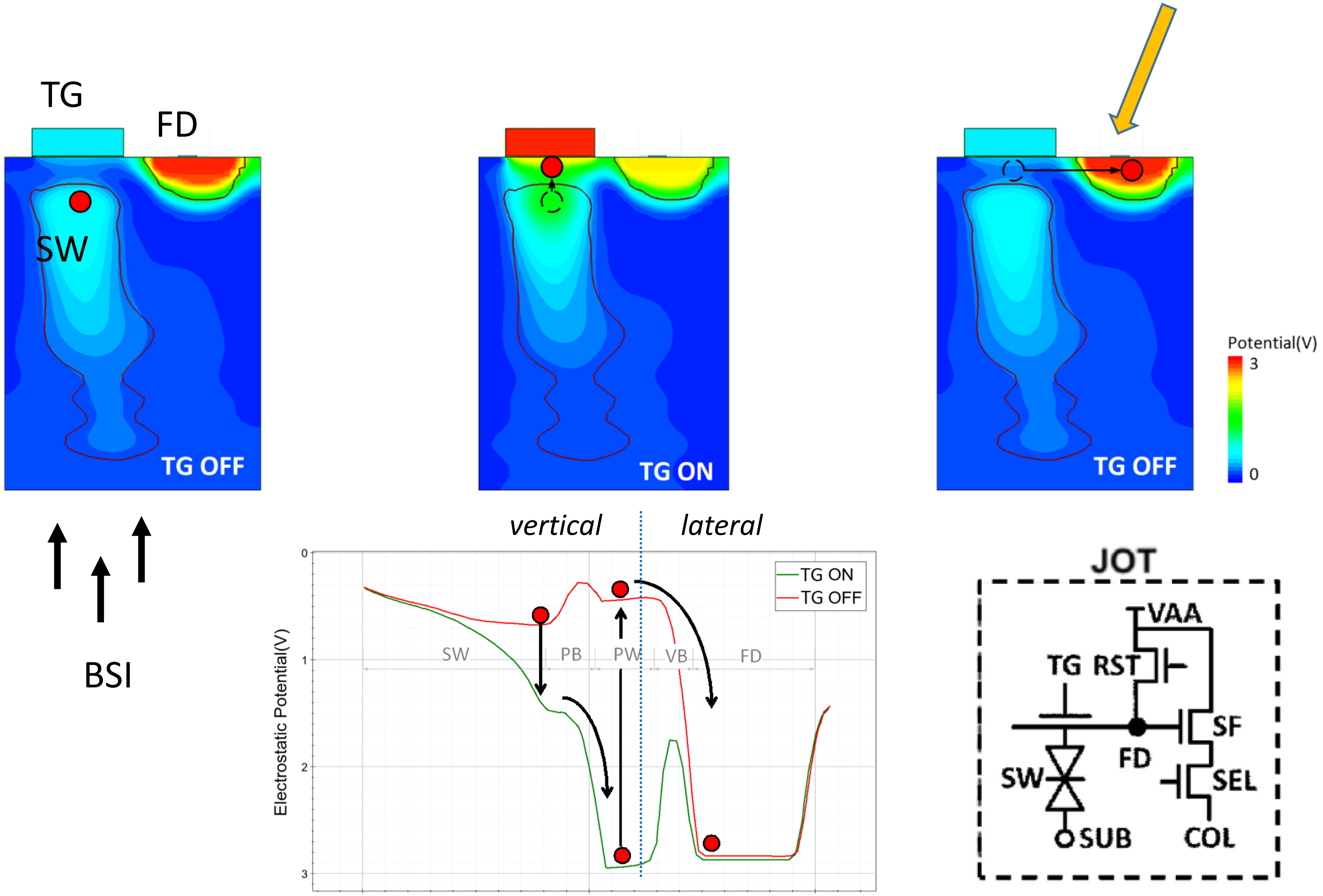
Integral under red curve to the right of U_T

Poisson distribution mass function

DARTMOUTH

Pump-Gate Jot: minimize TG-FD overlap capacitance

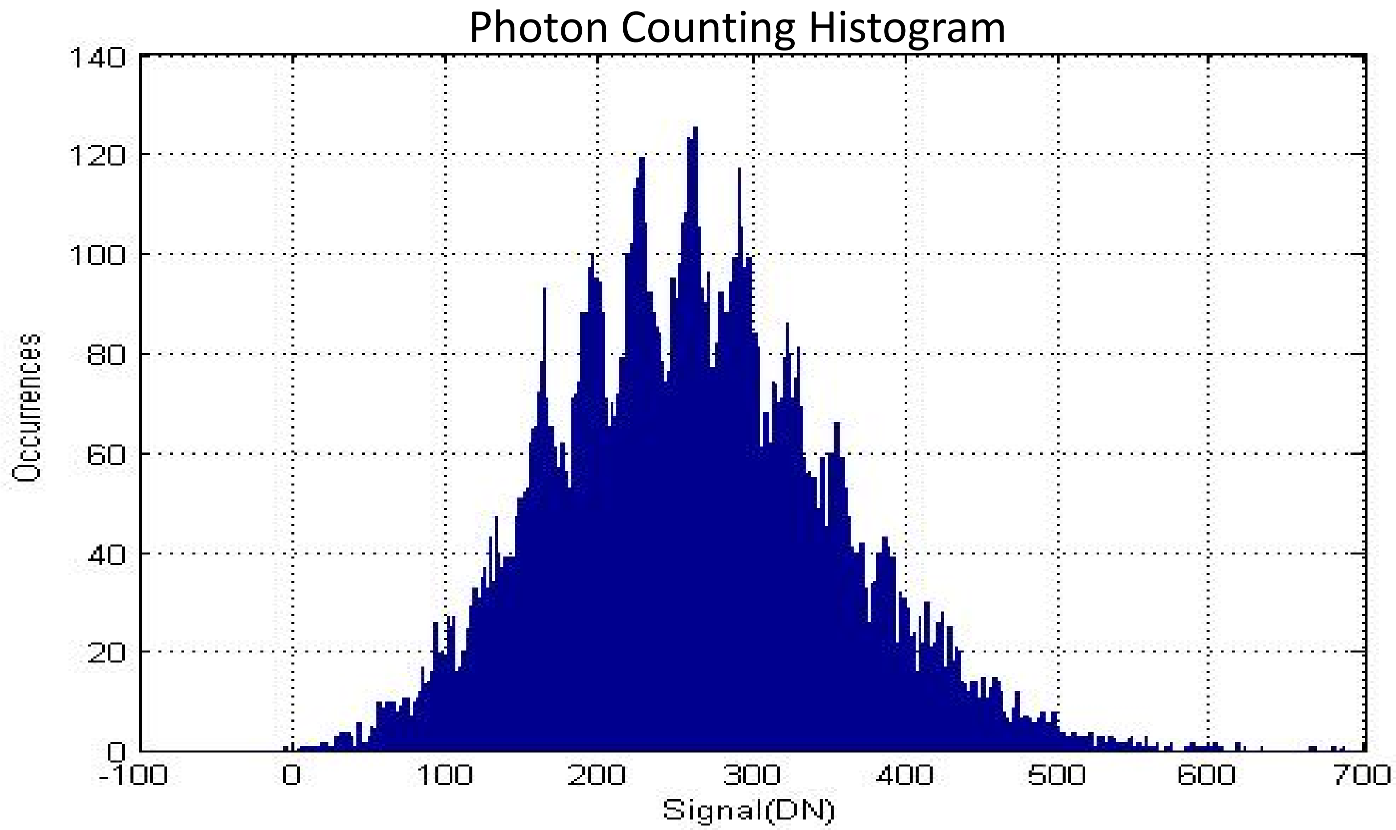
Highest possible CG
(Lowest possible cap.)



US Patent No. 9,728,565 B2
Fossum, Ma, Hondongwa

First observation of quantization of signal electrons in CMOS image sensor (Room temperature, single read, no avalanche)

DARTMOUTH

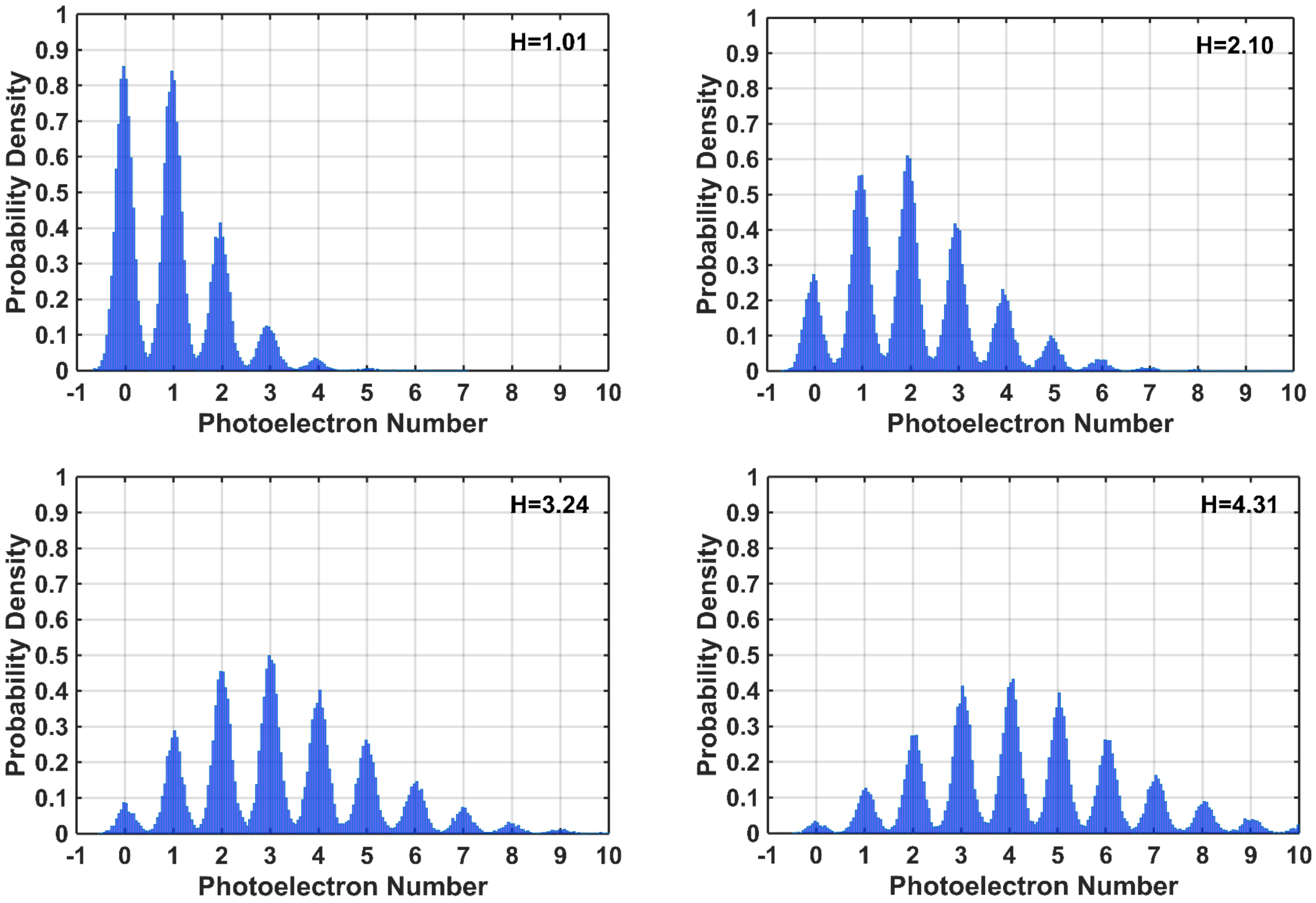


Ma and Fossum, Dartmouth College June 2015. Presented at IISW June 2015

https://imagesensors.org/wp-content/uploads/2016/03/2015-June-IISW-Multibit-QIS.pdf

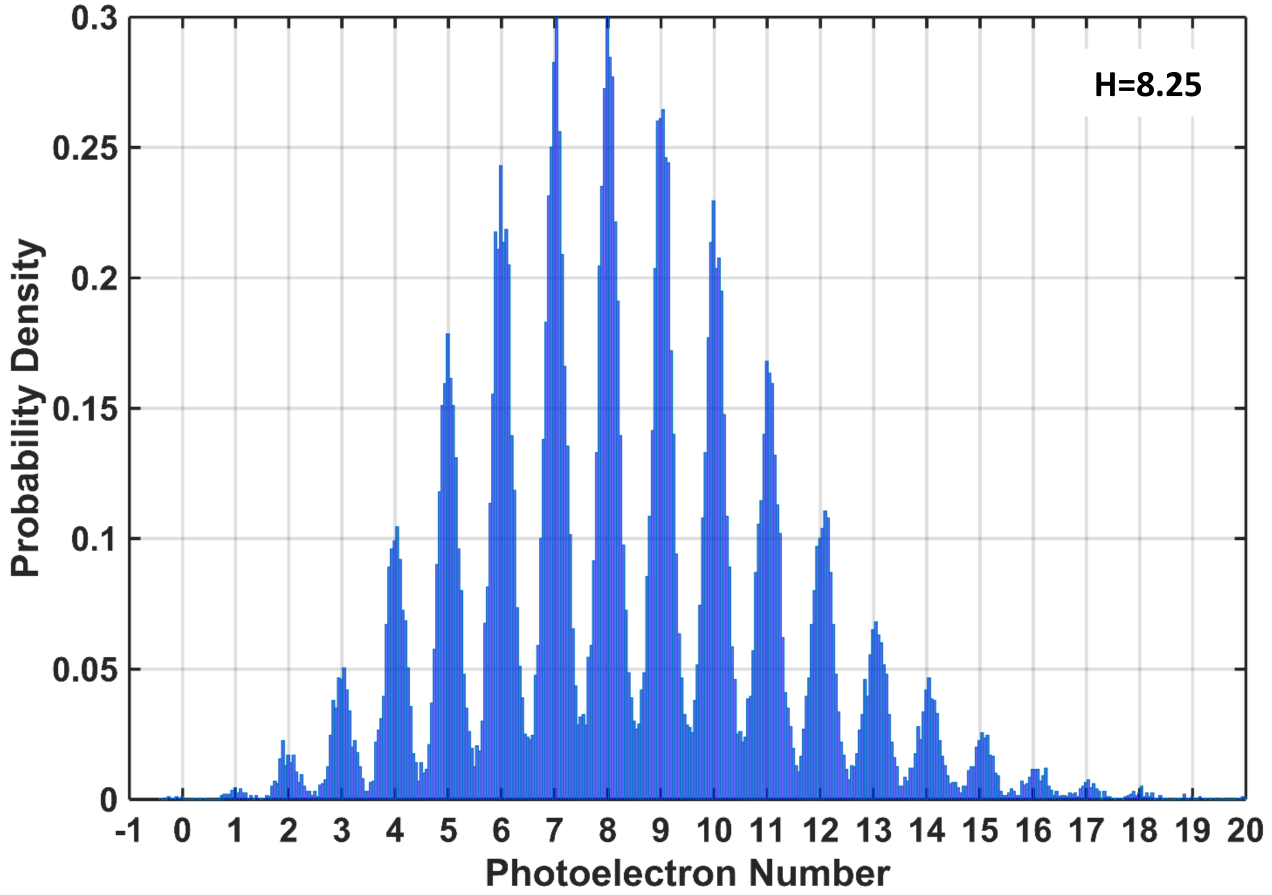
Photon Counting Histogram for "a Golden Pixel" Experimental Data

20k reads of same jot, 0.175e- rms read noise ~21DN/e- (61.2uV rms 350uV/e- or 0.45fF)
Room temperature, no avalanche, 20 CMS cycles, jot:TPG PTR BC



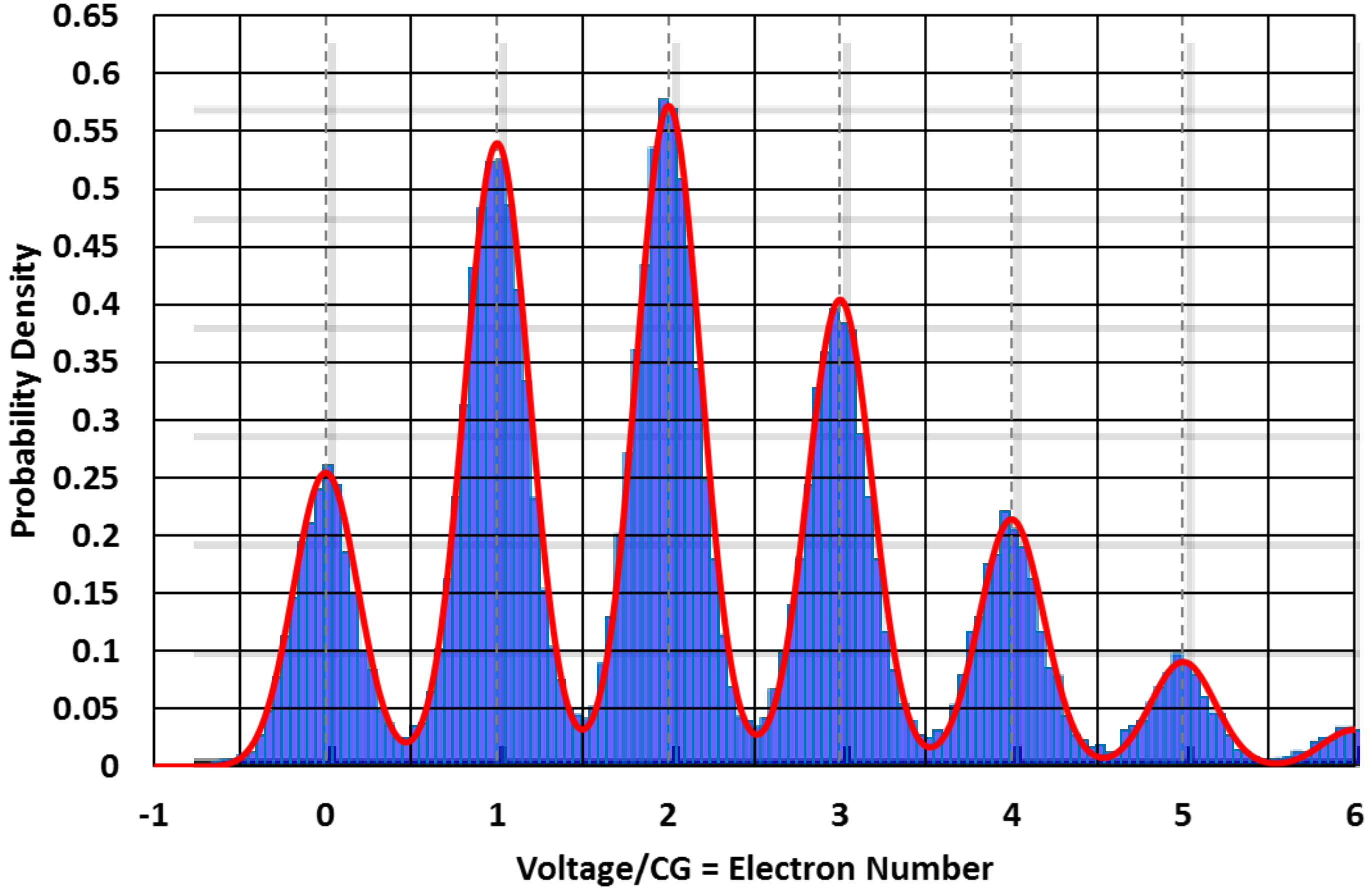
Experimental Data - Photon Counting Histograms

20k reads of same jot, 0.20e- rms read noise ~21DN/e-
Room temperature, no avalanche, 20 CMS cycles, jot:TPG PTR BC



Model vs. Data = New characterization tools

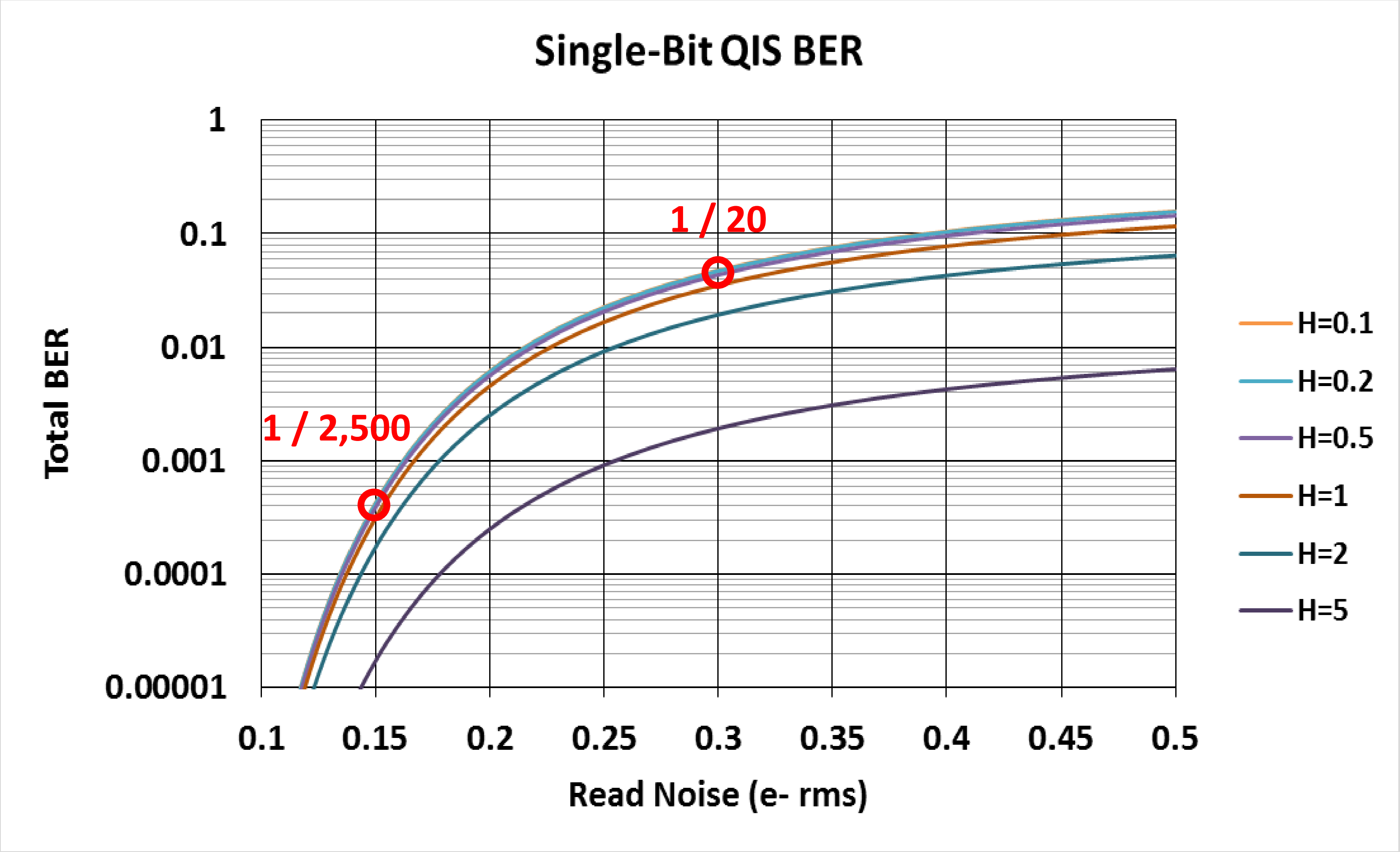
Conversion gain from peak spacing

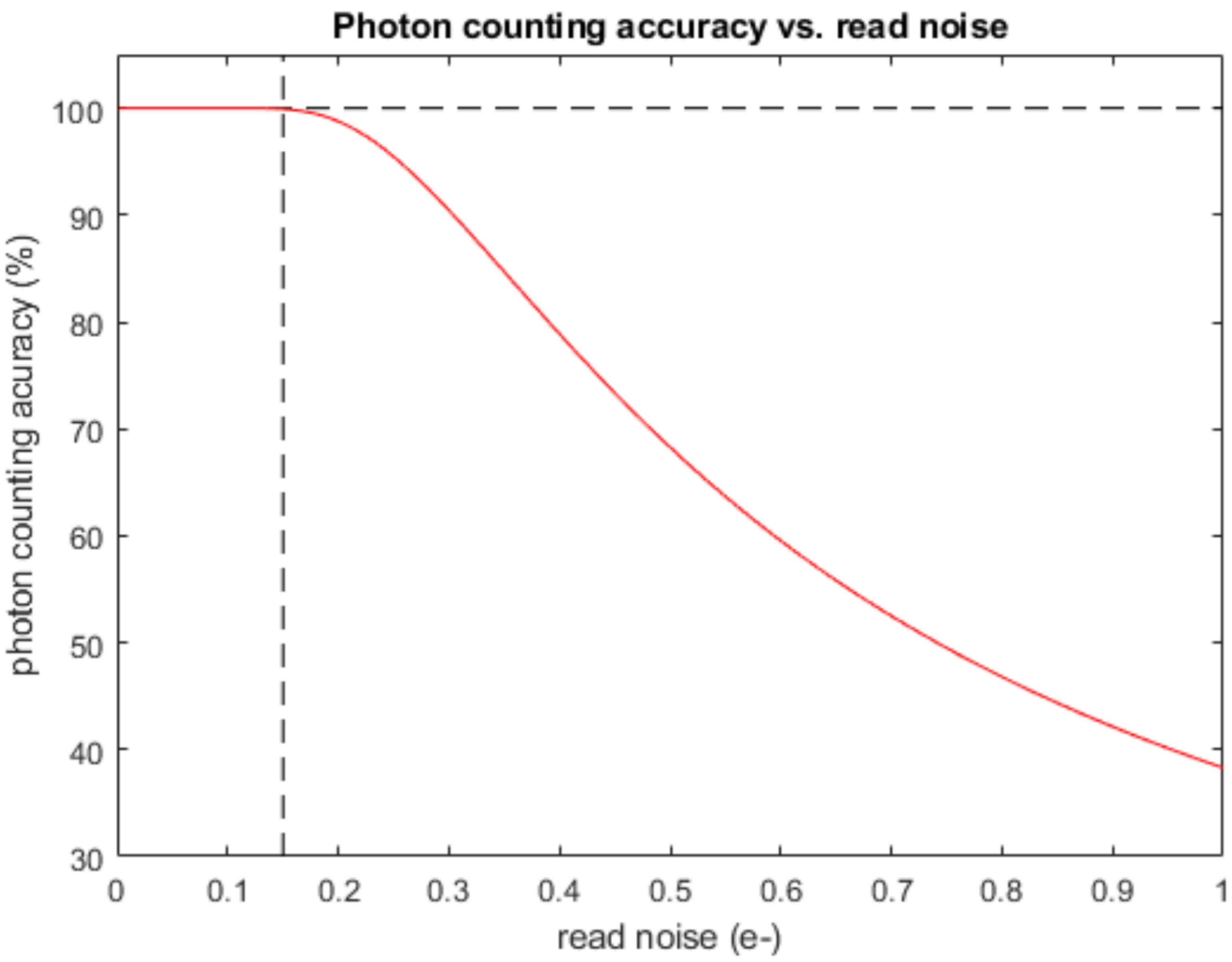


Quanta exposure from relative peak heights

Read noise from valley-peak modulation value

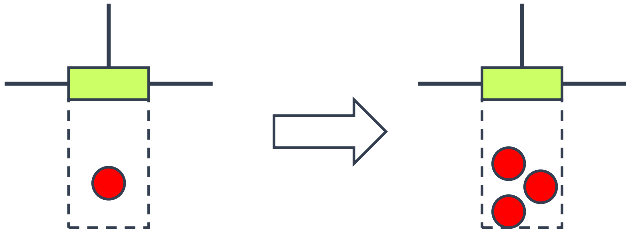
Bit error rate (BER) depends strongly on read noise





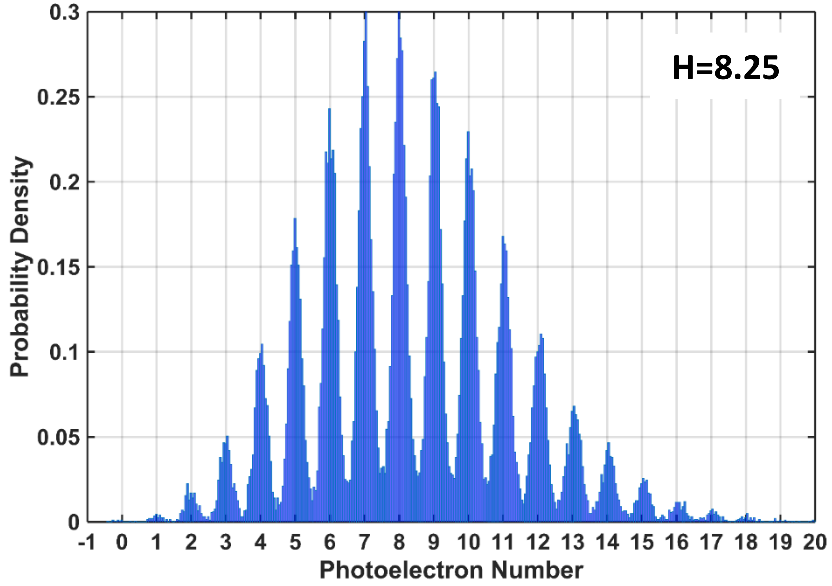
Posted on LinkedIn by **Aaron Hendrickson**, NAWC, Nov 16, 2023
Accuracy means probability that electron number read out is actual number

Multi-bit jot increases flux capacity and allows photon-number resolution

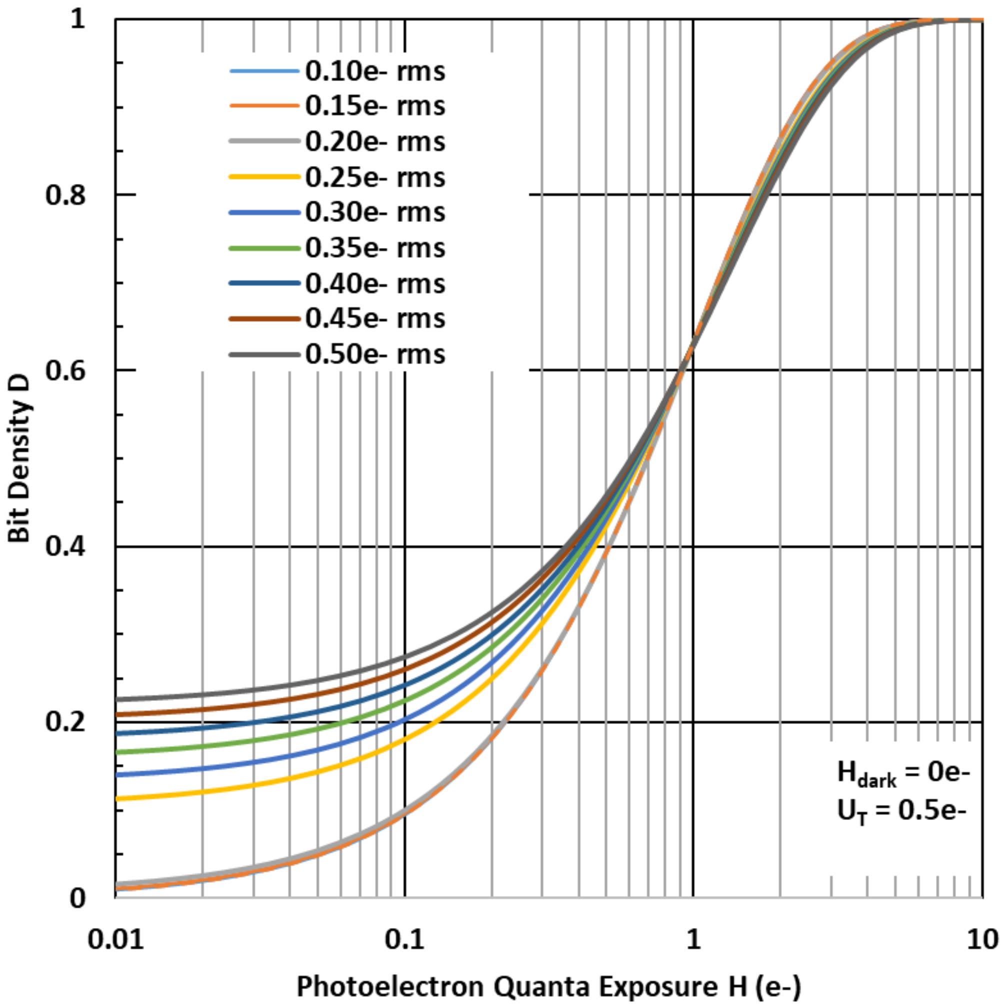


Single bit jot
0, 1 electrons

Multi-bit (2b) jot
0, 1, 2, 3 electrons

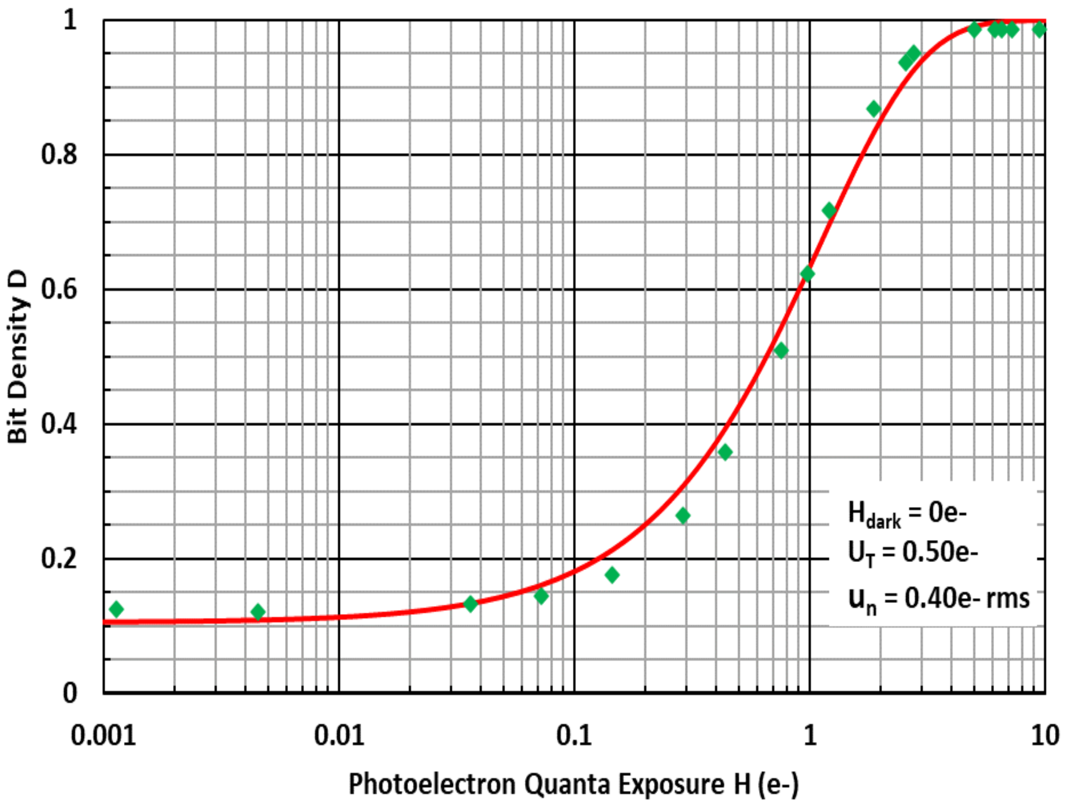


Effect of Read Noise on D-log H



E. R. Fossum, "Analog Read Noise and Quantizer Threshold Estimation From Quanta Image Sensor Bit Density," in IEEE Journal of the Electron Devices Society, vol. 10, pp. 269-274, 2022, doi: 10.1109/JEDS.2022.3157785.

From 1bQIS binary data, one can estimate read noise

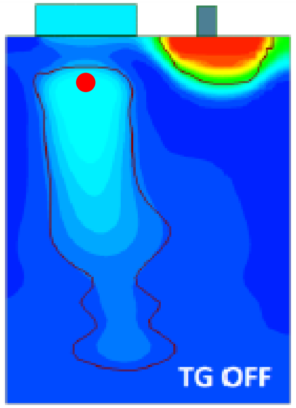


Read noise and quantizer threshold estimated to within a few hundredths of an electron!

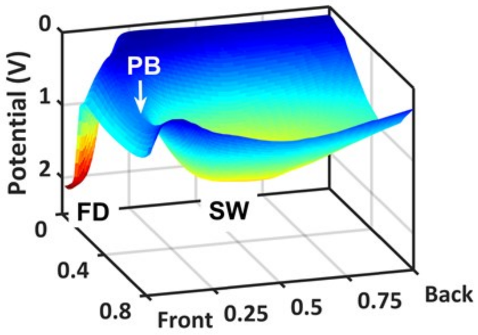
E. R. Fossum, "Analog Read Noise and Quantizer Threshold Estimation From Quanta Image Sensor Bit Density," in IEEE Journal of the Electron Devices Society, vol. 10, pp. 269-274, 2022, doi: 10.1109/JEDS.2022.3157785.

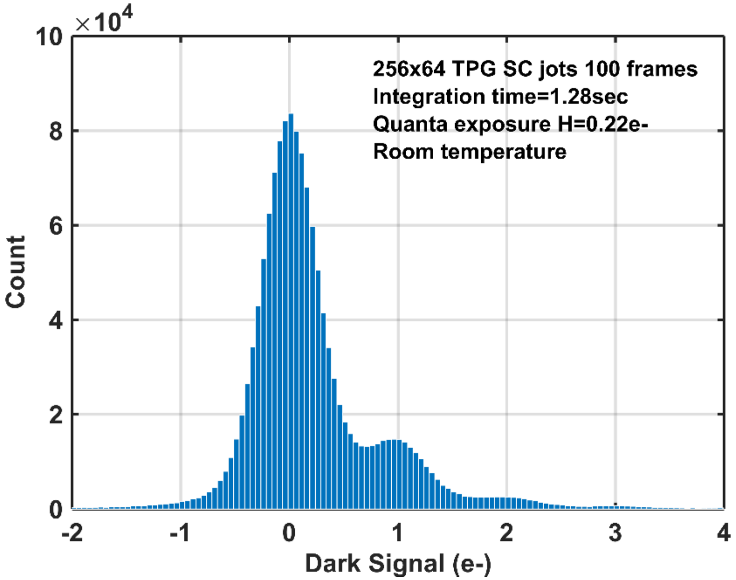
Very low dark current (0.07 cps at RT)

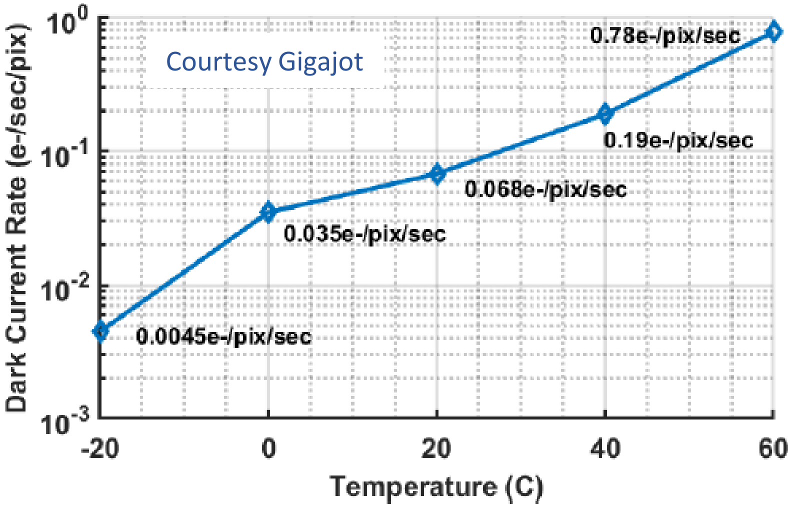
Room Temp: ~0.07e-/s avg. (~1pA/cm²)
Previously measured ~2x every 10C



Storage well isolated from surface

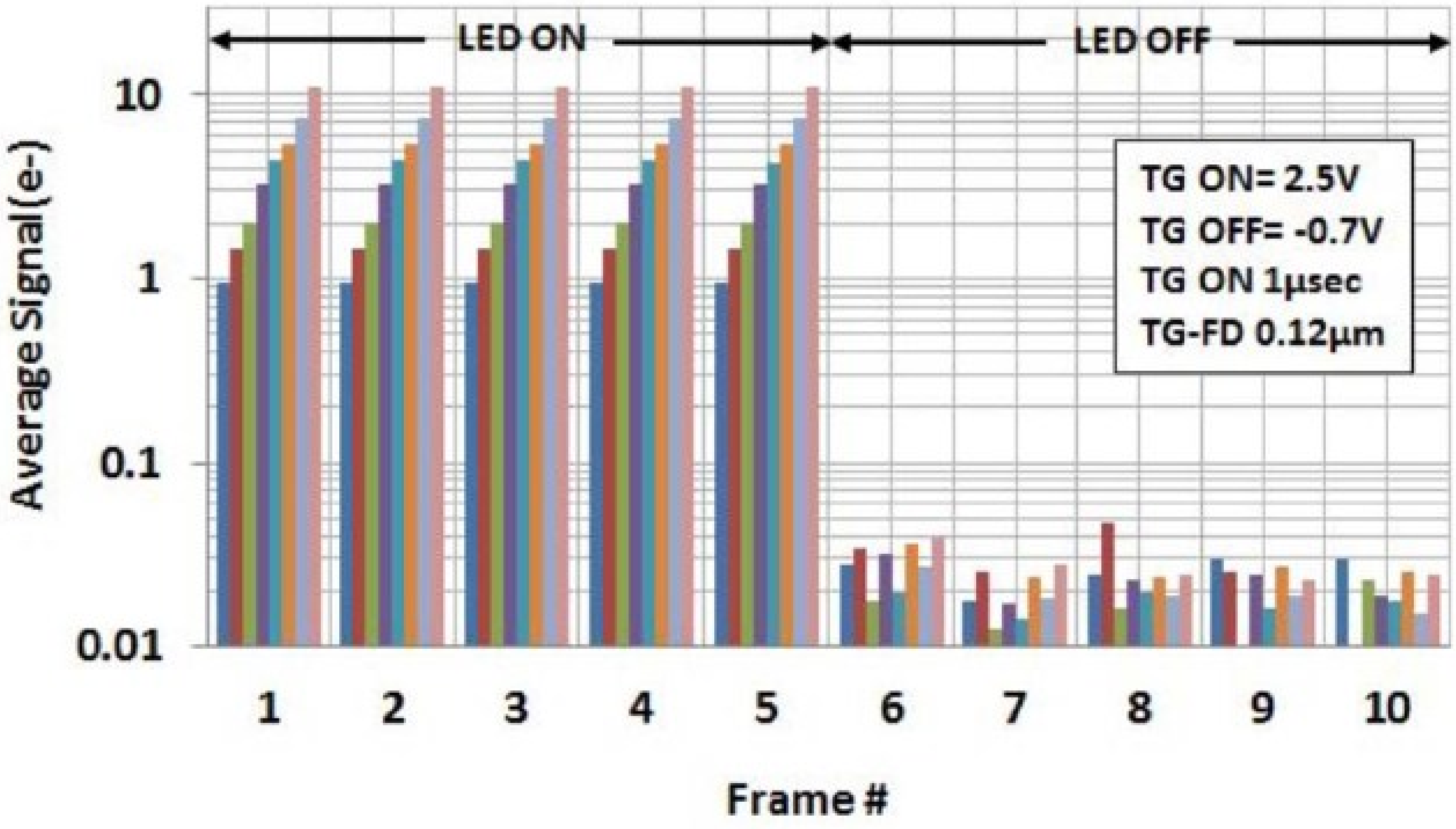






Average Dark Current -20C to 60C

Negligible Lag



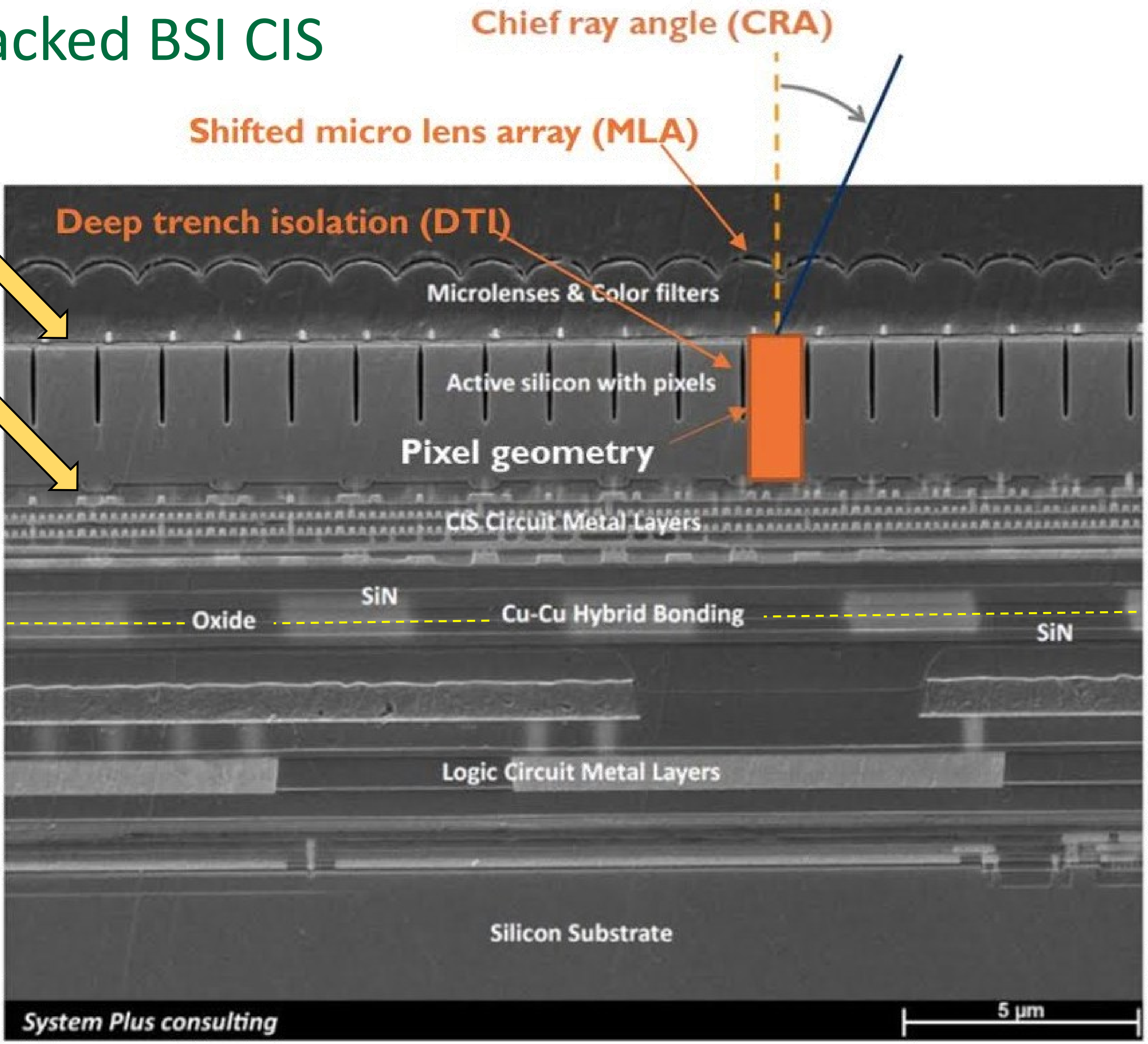
3D-stacked BSI CIS

"Backside" silicon surface

Readout "FD"

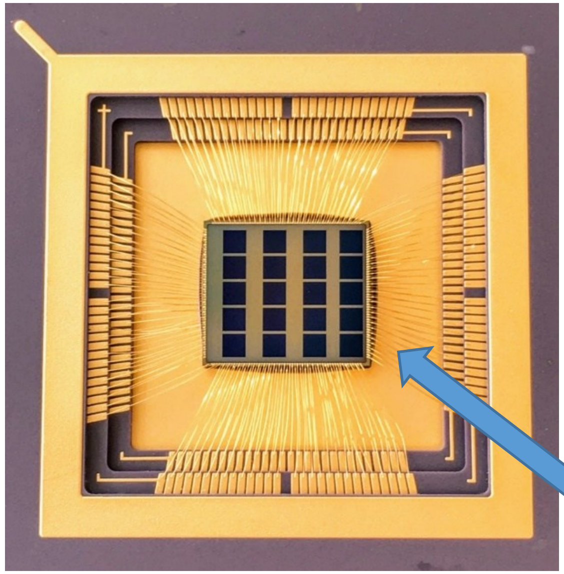
Detector wafer

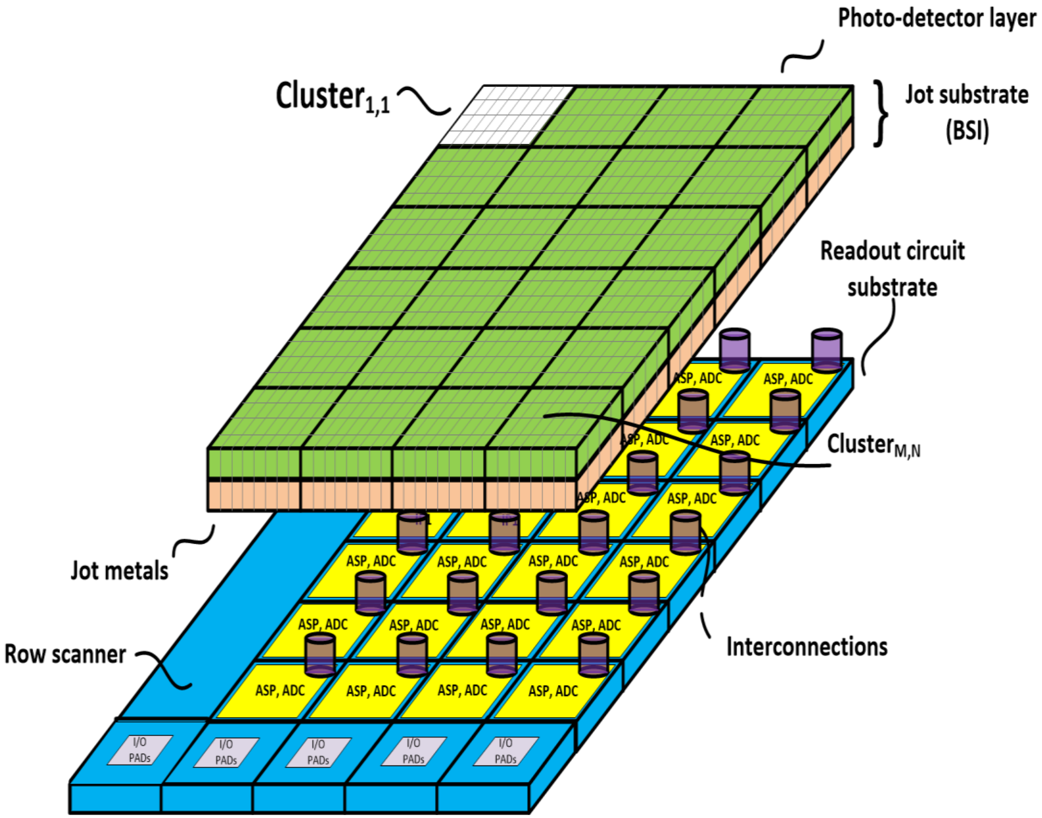
Logic wafer



20 Mpixel single-photon detector array

- Process technology: TSMC CMOS BSI 45nm/65nm 2-layer stacking
- Cluster parallel readout architecture for low power and modularity
- 20 different 1Mpixel arrays on test chip
- Readout Variation:
    - ➢ Analog
    - ➢ Single-bit Digital
- Pixel: 1.1µm 1024x1024
- Pixel variation: TPG, PTR, JFET





20 Mpixel single photon detector array

Summary of measured results
1Mpixel 1b QIS at room temp (2017)

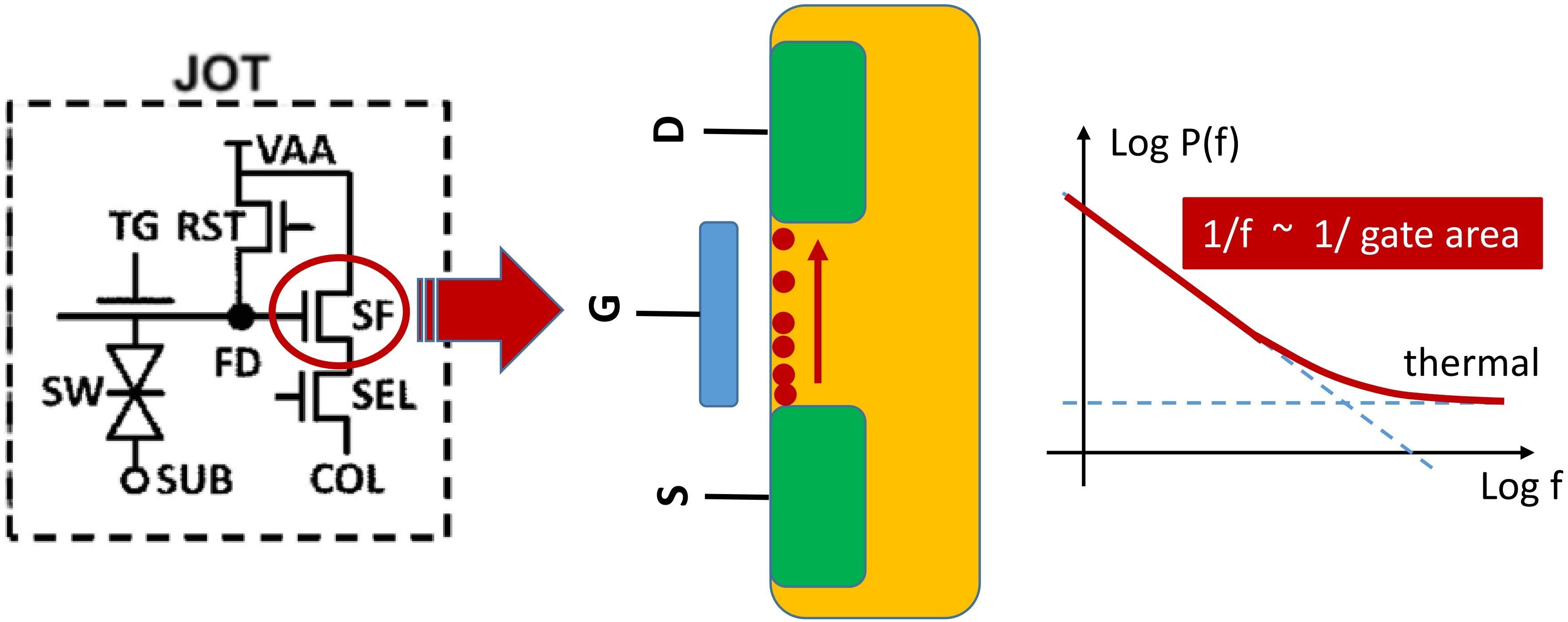
DARTMOUTH

Process	45nm (jot layer), 65nm (ASIC layer)
VDD	1.8V & 2.5V (Analog, digital and array), 3V & 2.2V (I/O pads)
Jot type	BSI Tapered Pump Gate 2-Way Shared RO
Jot pitch	1.1µm
BSI Fill Factor	~100%
Quantum Efficiency	79% @ 550nm
Conversion gain on column	345µV/e-
Input Referred Noise	0.22e- r.m.s.
Corresponding BER	~1%
Avg. Dark current (RT)	0.16e-/s
Equiv. Dark Count Rate (RT)	0.07Hz/jot

Equiv. PD Dead Time		<0.1%
Array		1024 (H) x 1024 (V)
Field rate		1040fps
ADC sampling rate		4MSa/s
ADC resolution		1 bit
Output data rate		32 (output pins) x 34Mb/s = 1090Mb/s
Package		PGA with 224 pins
Power	Array	2.3mW
	256 ADCs	7.5mW
	Addressing	4.1mW
	I/O pads	3.7mW
	Total	17.6mW
FOM ADC		6.9pJ/b

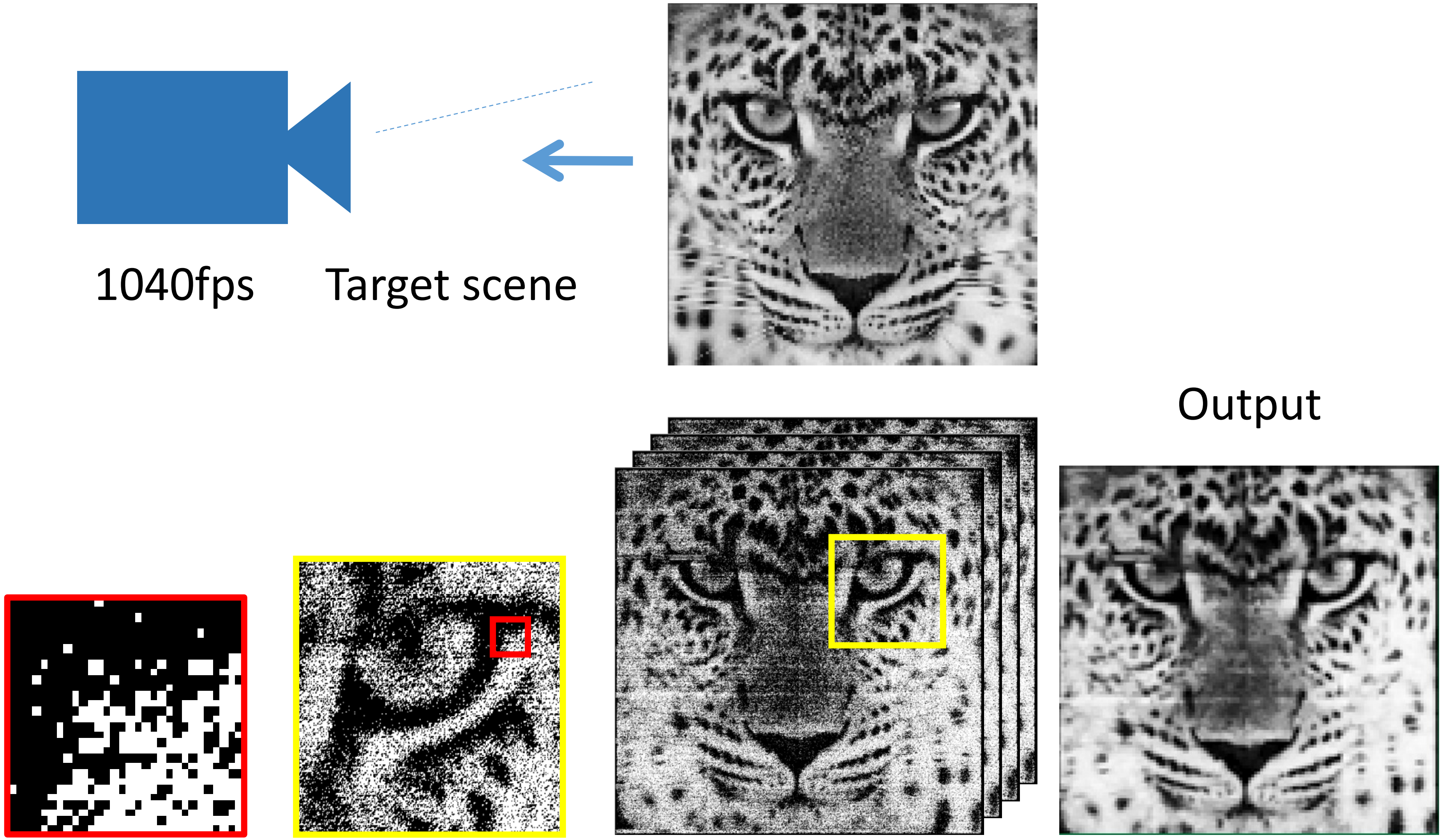
J. Ma, S. Masoodian, D. Starkey, E.R. Fossum, Photon-number-resolving megapixel image sensor at room temperature without avalanche gain, OSA Optica, vol. 4, no. 12, pp.1474-1481, December 2017. https://doi.org/10.1364/OPTICA.4.001474

Noise in first transistor is critical



- Bigger MOSFET gate, less voltage noise
- Bigger MOSFET gate, higher capacitance, lower CG, more input-referred noise

1Mjot prototype QIS experimental results (2017)



gigajot
WHERE EVERY PHOTON COUNTS

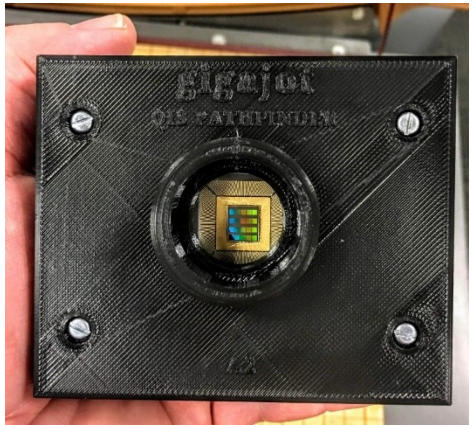
Gigajot Technology Inc. spinoff (2017)

Co-Founders


Saleh Masoodian

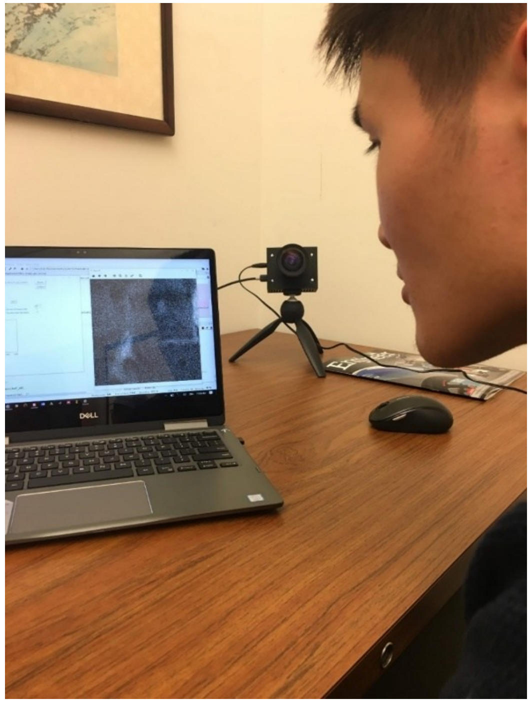

Jiaju Ma


Eric Fossum

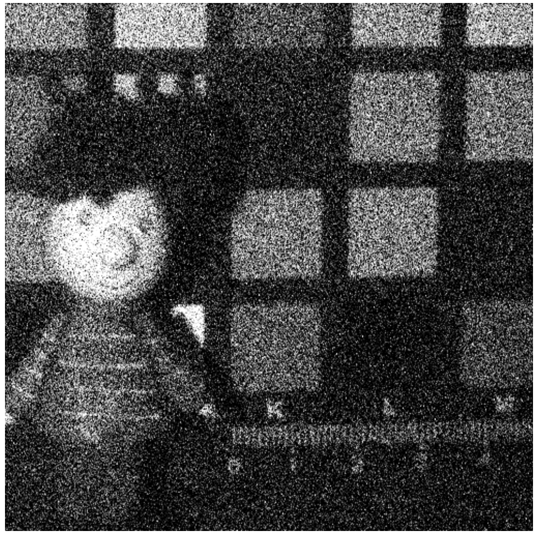


CIS-QIS technology great for low light, high resolution imaging and photon-number resolving systems

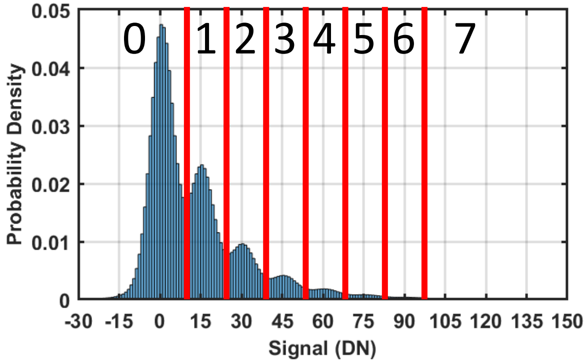
- Security systems
- Low light vision
- Internet of things (IOT)
- Biological imaging
- Astronomy
- Quantum Cryptography
- Photography
- Cinematography

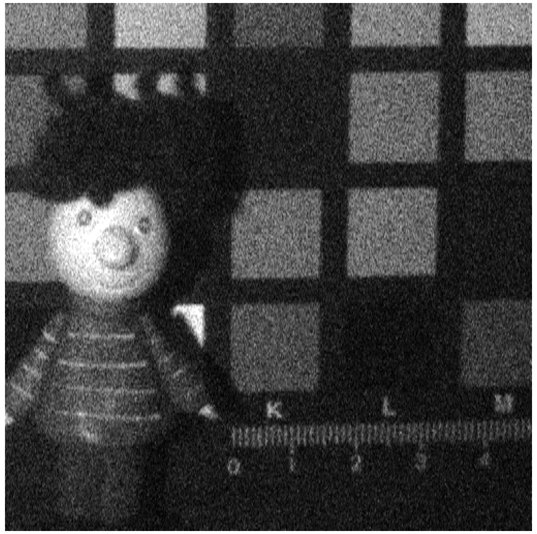


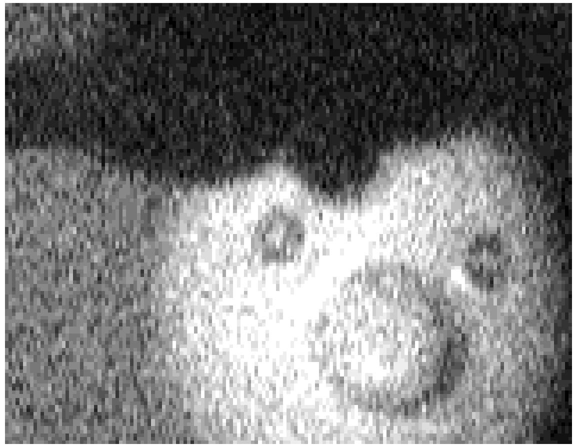
1Mpixel 3b QIS image with exposure of 0.87e-/pixel average



Raw image and Histogram







2x2x2 cubicle sum only

2x2x2 cubicle denoise

Images courtesy of Gigajot

gigajot
WHERE EVERY PHOTON COUNTS

A Photon-Counting 4Mpixel Stacked BSI Quanta Image Sensor with 0.3e- Read Noise and 100dB Single-Exposure Dynamic Range

Jiaju Ma, Dexue Zhang, Omar Elgendy, Saleh Masoodian
Gigajot Technology Inc., Pasadena, California, USA, email: jiaju.ma@gigajot.tech

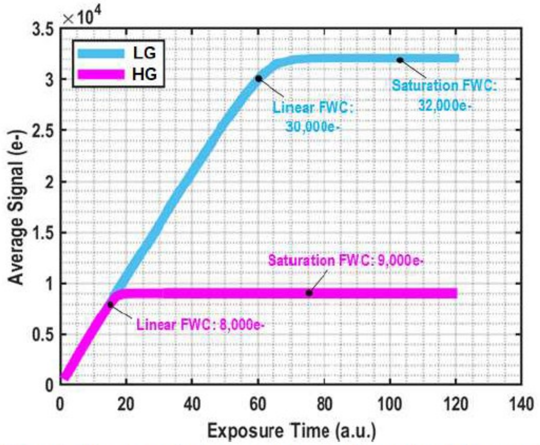


Fig. 4. Sensor photon response characteristics as a function of sensor exposure time in high-gain (HG) and low-gain (LG) modes.

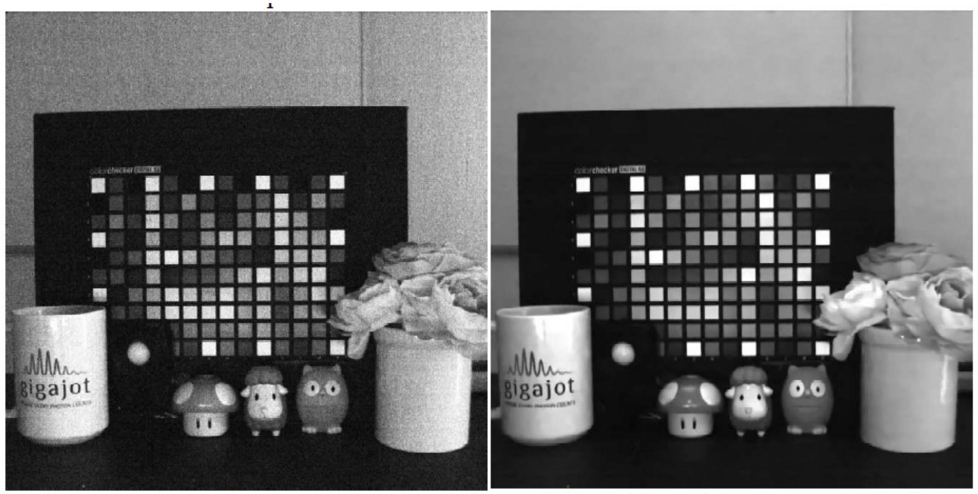


Fig. 5. Sample images under 0.03lux low-light condition with a f/1.8 lens, 8x PGA gain, and 30msec integration time. The raw image is shown on the left and the single-frame processed image enhanced by neural network is shown on the right.

Table 1. Sensor performance summary.

Fabrication Process	45nm BSI CIS/65nm Logic Stacked
Supply Voltage	3.0V/1.2V
Pixel Size	2.2um x 2.2um
Pixel Resolution	2048 x 2048
ADC Resolution	10/12/14 Programmable
Linear Full-Well Capacity	8,000e- (HG)
	30,000e- (LG)
Conversion Gain	200uV/e- (HG)
	39uV/e- (LG)
PRNU	1.0% (HG)
	0.8% (LG)
Read Noise	0.27e- RMS (@ peak, CMS x16)
	0.30e- RMS (@ median, CMS x16)
Vertical FPN	0.08e- RMS
QE peak	82% @ 480nm
Dynamic Range	100dB (@ HDR, single exposure)
Frame Rate	120fps (@ single gain, 12bit, CMS x1)
	60fps (@ dual gain, 12bit, CMS x1)
Power Consumption	550mW @ 120fps

Fig. 6. Sample images with high-gain mode on the left and HDR mode on the right. The HDR mode can capture both outdoor and indoor scenes across about 95dB dynamic range, but the outdoor scene is saturated with the high-gain mode.

2021 Symposium on VLSI Circuits Digest of Technical Papers

16.7Mpix CIS-QIS by Gigajot

gigajot
WHERE EVERY PHOTON COUNTS

2021

IEEE ELECTRON DEVICE LETTERS, VOL. 42, NO. 6, JUNE 2021 891

A 0.19e- rms Read Noise 16.7Mpixel Stacked Quanta Image Sensor With 1.1 μm-Pitch Backside Illuminated Pixels

Jiaju Ma, *Member, IEEE*, Dexue Zhang, Omar A. Elgendy, *Member, IEEE*, and Saleh Masoodian

TABLE I
SENSOR PERFORMANCE SUMMARY

Process Technology		45nm/65nm Stacked CIS BSI Process
Pixel Size		1.1 µm x 1.1 µm
Pixel Resolution		4096 x 4096
Chroma		RGB Bayer /Mono
Power Consumption		600 mW
ADC Bit Depth		1-14 bit programmable
Max Frame Rate		40 fps @ 4096 x 4096
		60 fps @ 3840 x 2160
Read Noise	25 °C, CMS 8	0.19 e- rms @ Peak 0.22 e- rms @ Median
	-20 °C, CMS 8	0.17 e- rms @ Peak 0.20 e- rms @ Median
RTS (>10e- rms)		<1 ppm
Linear Full-Well Capacity		1500 e-
Dynamic Range		77 dB
Non-Linearity		<0.5%
PRNU		<1.5%
Quantum Efficiency @ Peak		76% @ 520nm
Dark Current	60C	4.5 e-/pix/sec
	20C	0.086 e-/pix/sec
Lag		<0.1 e- (less than the measurable level)

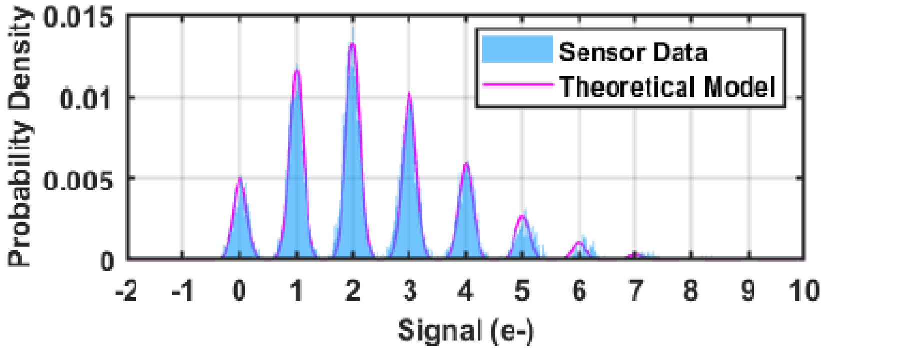
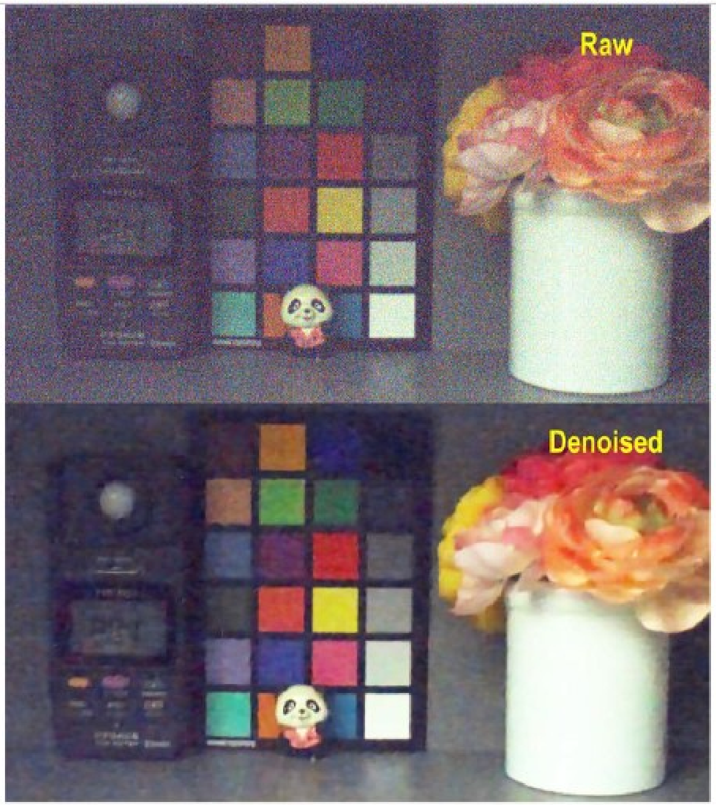
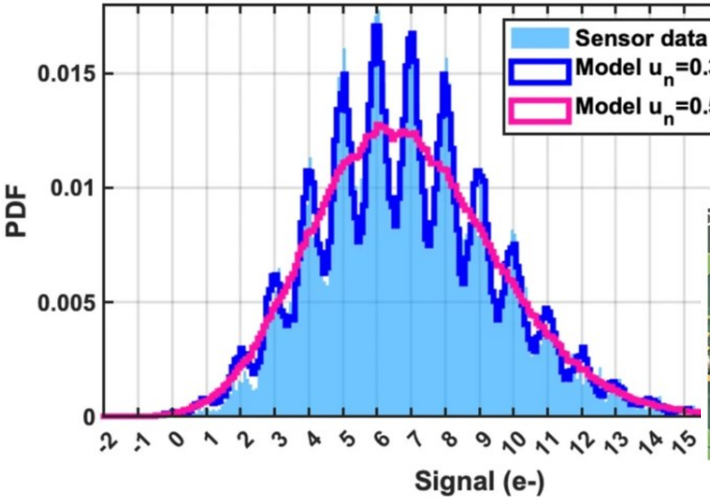


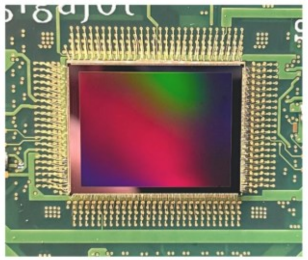
Fig. 1. A photon-counting histogram from a pixel with 0.12 e- rms read noise and 2.3 e-/pixel average signal level showing a distinctly

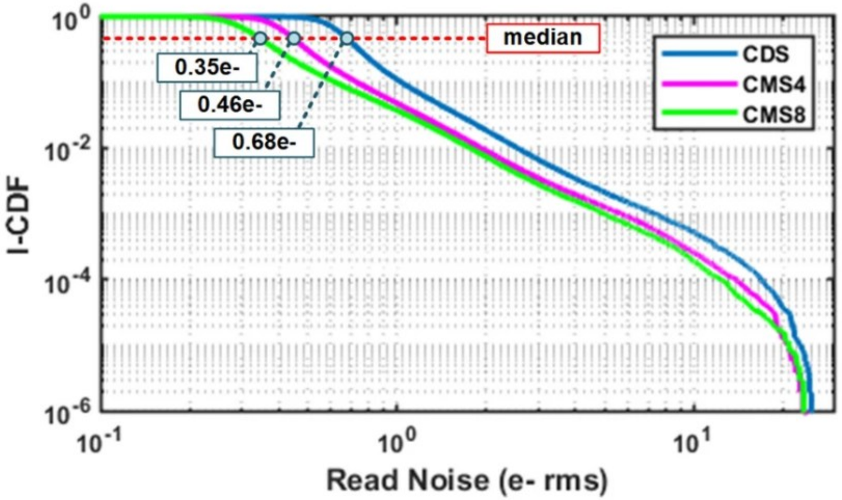


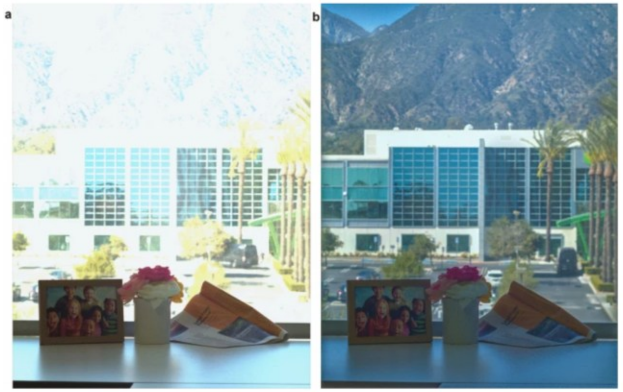
0.01 lux, f/1.4 600msec

163 Mpixel CIS-QIS with photon-number resolution and high dynamic range (2022)

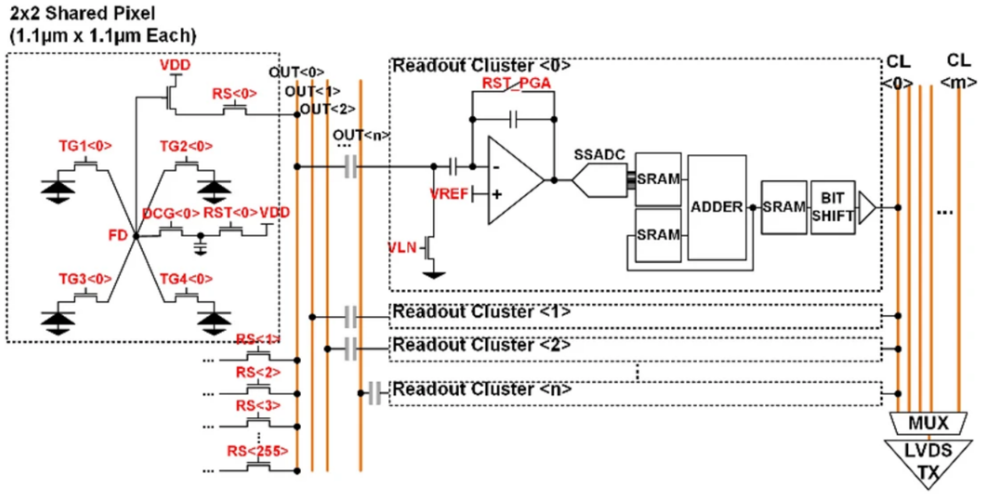








Sample images under HDR condition with and without DPG operation. The sample images were taken 2 × 2 binning with a F/8.0 lens and 100 ms exposure time. (**a**) HCG only. (**b**) DPG mode.



Ma, J., Zhang, D., Robledo, D. *et al.* Ultra-high-resolution quanta image sensor with reliable photon-number-resolving and high dynamic range capabilities. *Nature Sci Rep* **12**, 13869 (2022). https://doi.org/10.1038/s41598-022-17952-z OPEN ACCESS

Recent 3.2Mpix SPAD-QIS by Canon

Canon

Megapixel 3D-Stacked Charge Focusing SPAD for Low-Light Imaging and Depth Sensing

2021 IEEE IEDM Dec. 2021

K. Morimoto*, J. Iwata*, M. Shinohara, H. Sekine, A. Abdelghafar, H. Tsuchiya, Y. Kuroda, K. Tojima, W. Endo, Y. Maehashi, Y. Ota, T. Sasago, S. Maekawa, S. Hikosaka, T. Kanou, A. Kato, T. Tezuka, S. Yoshizaki, T. Ogawa, K. Uehira, A. Ehara, F. Inui, Y. Matsuno, K. Sakurai, and T. Ichikawa

$$\left(\frac{6.39}{1.1}\right)^2 = 33.8$$

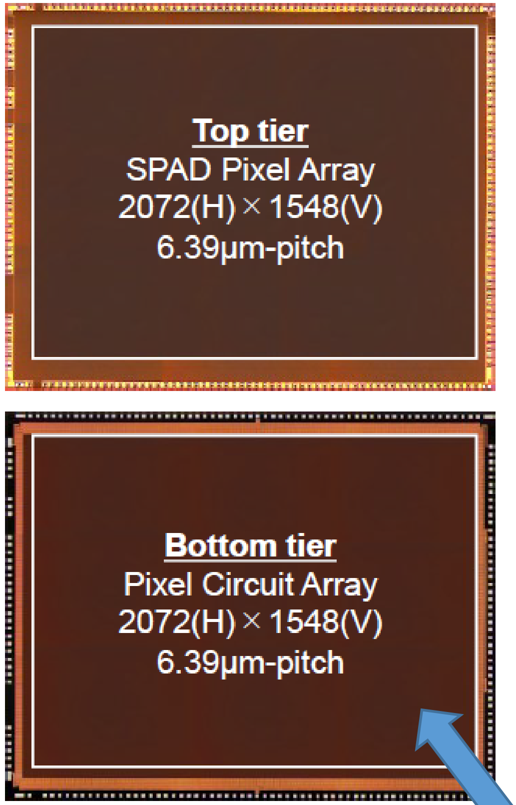


Fig. 13. Chip micrographs of prototype 3D-stacked BSI SPAD image sensor.

11b per-pixel counter

	This work
Sensor architecture	Charge focusing SPAD
Process technology	90nm/40nm 3D-BSI
Pixel pitch (µm)	6.39
Pixel array size	2,072 × 1,548
Read noise (e^-_{rms})	0
Frame rate (fps)	60
VB (V)	30
Fill factor (%)	~100
Max PDE (%)	69.4 (V_{ex}=2.5V)
PDE at 940nm (%)	24.4 (V_{ex}=2.5V)
Median DCR*1 (cps)	1.8 (V_{ex}=2.5V)
DCR per area*2 (cps/µm²)	0.044 (V_{ex}=2.5V)
Timing jitter FWHM (ps)	100 (V_{ex}=2.5V)

*1At room temperature (25°C) *2Normali

Table 1. Performance sumr

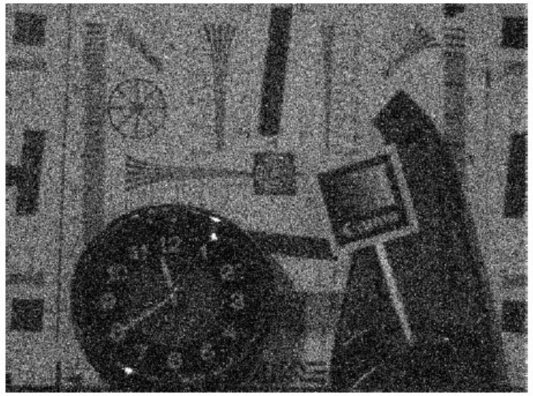


Fig. 6. Monochrome intensity image captured by 3.2 megapixel SPAD imager under scene illuminance of 0.3mlux (w/o post-processing).

Fig. 4. Full-resolution color intensity image captured by prototype 3.2 megapixel SPAD image sensor under high light.

DARTMOUTH

Examples of CIS-QIS and SPAD-QIS Progress

Year	Who	Type	3D BSI	LV	Depth 1b/mb	Pitch (μm)	Res. (Mpix)	FPS (fps)	Power (mW)	RT DCR (e-/s)	QE/ PDE
2014	Edin./ST	SPAD			1b	8.0	0.077	5,000	69	312	-
2014	EPFL	SPAD			1b	24.0	0.065	156,000	1650	350	14%
2015	MIT/LL	SPAD			1b/mb-7	25.0	0.065	8,000	-	>1000	-
2015	Dartmouth	CIS		✓	Analog	1.1	0.001	n/a	n/a	<1	-
2016	Edin.ST	SPAD	✓		mb-12	7.83	0.015	500	70	<200	12%
2017	Dartmouth	CIS	✓	✓	1b	1.1	1.0x20	1,000	19	<1	80%
2019	EPFL	SPAD			1b	16.4	0.262	97,700	700	7.5	-
2019	Edin./ST/HWU	SPAD	✓		mb-14	9.2	0.065	30	78	20	23%
2019	Panasonic	VAPD			1b	6.0	0.160	60	-	100	-
2020	Canon/EPFL	SPAD			1b	9.4	0.5x2	24,000	1070	2	3.6%
2021	Canon	SPAD	✓		mb-11	6.4	3.2	60	-	1.8	69%
2021	Sony	SPAD-	✓		mb-9	12.2	0.042	60	-	35	62%
2021	FBK	SPAD			1b	7.0	0.0002	-	-	>1000	-
2021	Gigajot	CIS	✓	✓	mb-12	2.2	4.194	60	550	0.2	84%
2021	Gigajot	CIS	✓	✓	mb-12	1.1	16.777	30	600	0.02	80%
2022	Gigajot/Dart	CIS	✓	✓	1b	1.1	2.097	500	68	<1	80%
2022	Gigajot	CIS	✓	✓	mb-14	1.1	162.9	7.5	3860	1.35@60C	87%

Also Hamamatsu qCMOS (CIS) and BAE Fairchild sensor (CIS)

J. Ma, S. Chan and E. R. Fossum, "Review of Quanta Image Sensors for Ultralow-Light Imaging," in IEEE Transactions on Electron Devices, vol. 69, no. 6, pp. 2824-2839, June 2022, doi: 10.1109/TED.2022.3166716.

DARTMOUTH

Broad Comparison

CIS QIS	SPAD QIS
Smaller pixel size, higher resolution and/or lower cost	No read noise or threshold uniformity worries.
Consumer application possible	Dual mode – ToF and QIS
Benefits from CIS pixel platform shrink	Major engineering for each new generation shrink
Lower power	Benefits more from digital circuit shrink but power high for higher flux conditions
Photon number resolution by ADC on signal AFTER integration	Photon number resolution by digitally pulsing a counter in an always-on circuit
Gated operation possible	Faster gated operation possible
	Very fast response to photon arrival due to instant gain

DARTMOUTH

Challenges for QIS

CIS-QIS

- Improvement in read noise tail.
- 2X Pixel shrink to 0.5um without input-referred noise increase
- Reduced power dissipation by 10x.
- Killer app

SPAD-QIS

- 10x Pixel shrink to sub-micron size
- Resolution increase
- Reduction of power, esp. under higher flux
- Continued improvement in dark count
- Continued improvement in photon detection efficiency
- Killer app

DARTMOUTH

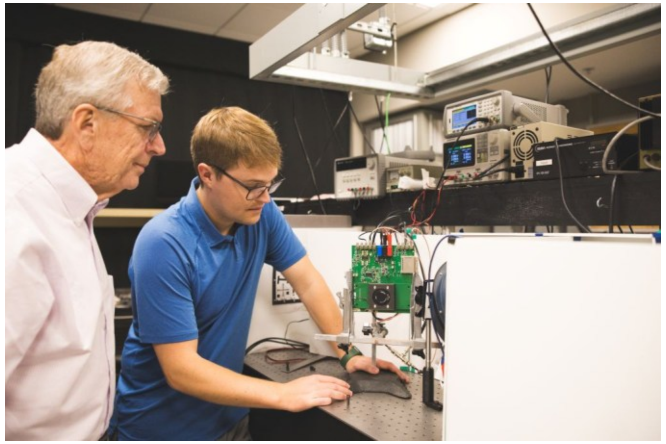
QIS Conclusions

- Deep sub-electron read noise enables photon-counting and photon-number resolution in visible light range using CIS approach
- Fabricated in almost standard CMOS image sensor foundry process
- Operates at room temperature with ~1um or less pixel pitch

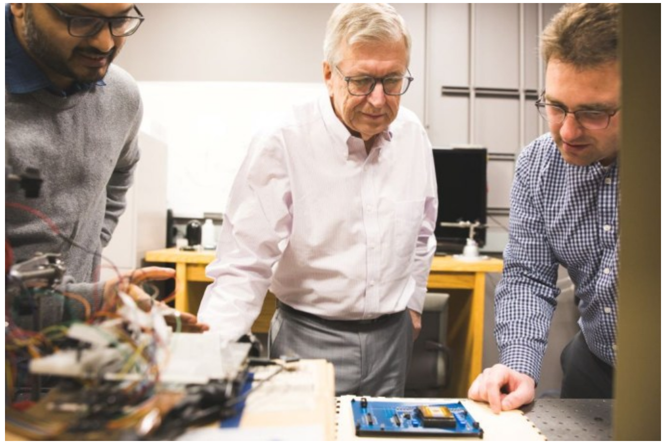
Near future:

- Probably CIS QIS technology combined into CIS mainstream
- SPAD QIS also has a bright future

Current activities in my lab at Dartmouth

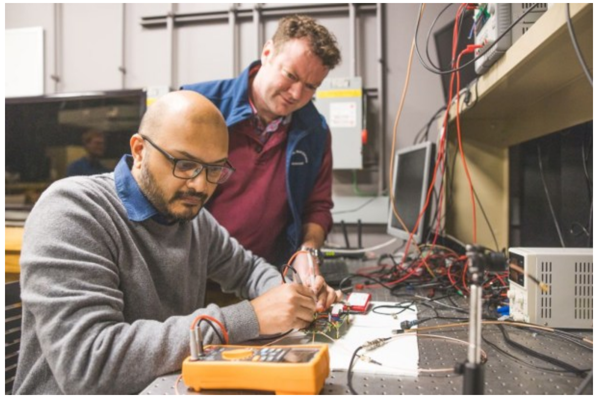


Nicholas Shade



Karthik Venkatesan and Joe Lazzaro

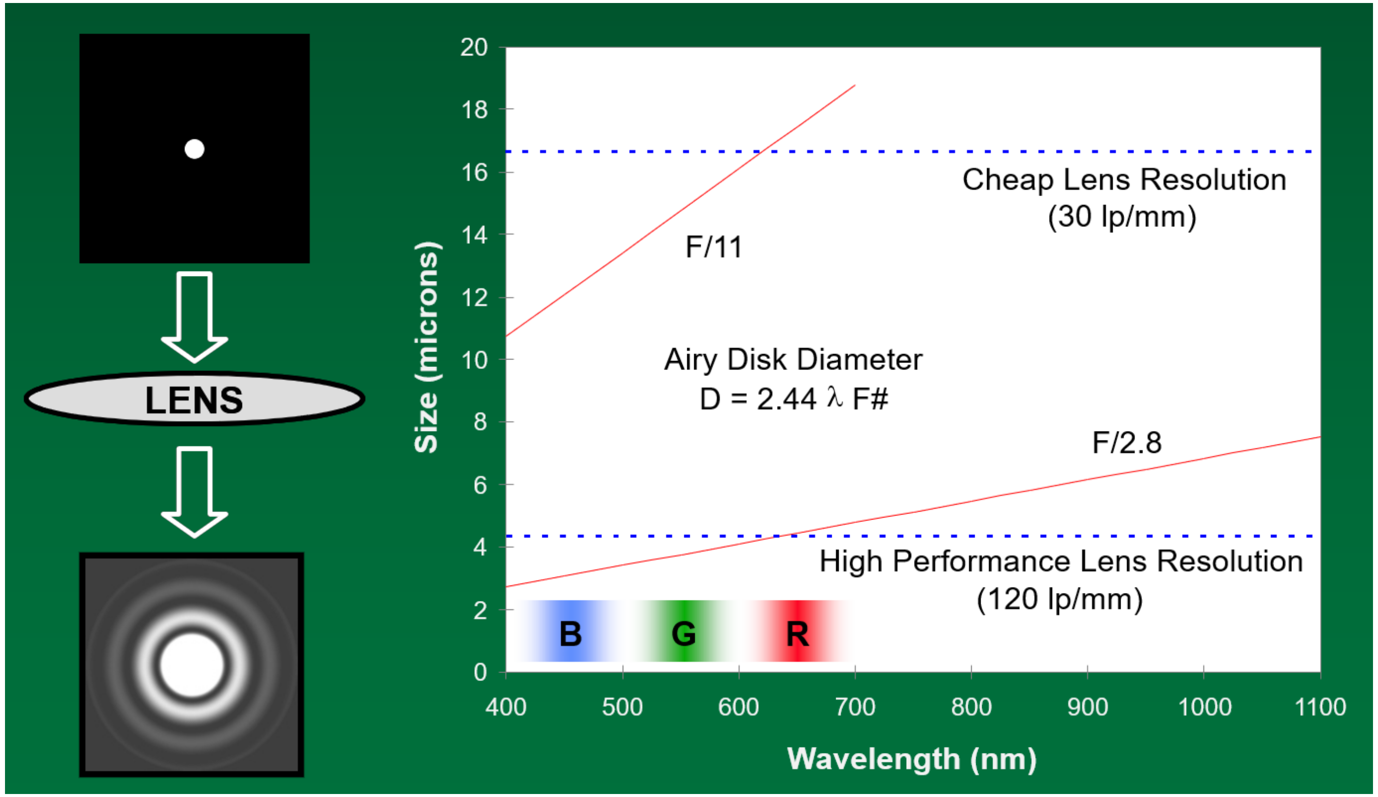
- Photon-counting image sensors for space
- Time-gated image sensors for HDR bio-med apps
- HDR sensors for wearable biosensing
- Laser communications in free space
- Revisit "Skipper-in-CMOS" 30+ years later



Karthik Venkatesan and John Doherty

Future Challenge – Beat Conventional Diffraction Limit

Some combination of pixel level optics and computational imaging so effective pixel pitch scales with technology node and not limited by conventional optics laws.
Of course, photon number per pixel will limit corrections due to noise.



Reading List

- Active Pixel Sensors: Are CCDs Dinosaurs? 1993
  - https://doi.org/10.1117/12.148585
- CMOS Image Sensors: Electronic Camera-on-a-Chip 1997
  - https://ieeexplore.ieee.org/abstract/document/628824
- Quanta Image Sensors – Every Photon Counts 2016
  - https://doi.org/10.3390/s16081260
- Review of Quanta Image Sensors for Ultralow-Light Imaging 2022
  - https://ieeexplore.ieee.org/document/9768129
- Digital Image Sensor Evolution and New Frontiers 2024
  - https://www.annualreviews.org/content/journals/10.1146/annurev-vision-101322-105538