The Big Picture: CMOS Image Sensors
From Zero to Billions and Beyond

Eric R. Fossum
EECS Colloquium
University of California at Berkeley
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CMOS Image Sensors Enable Billions of Cameras Each Year
Many kinds of digital cameras

Photography
- Camera phone
- Digital single lens reflex (DSLR)
- Mirrorless and Point-and-shoot

Video
- TV (0.3Mpix), HDTV (2Mpix) UDTV (133Mpixel)
- Webcam
- High speed – slow motion
- Motion capture
- Glass
- Body cam

Medical
- Endoscopy
- Pill camera
- Dental X-rays

Machine Vision
- Automotive
- Security
- Inspection

3D ranging
- Gesture control

Etc.
Inventions
“Necessity is the Mother of Invention”

Voyager (1977) ISS had vidicon cameras (wide angle and narrow angle)

Mass: 38.2 kg
Power (avg): 35.0 W
MOS “Photomatrices” 0th Generation Image Sensor

~June 1966

First self-scanned → Sensor 10x10 1966/67

Mid-late 1960’s MOS arrays at Plessey with startup Integrated Photomatrix Ltd. (IPL)

The 64 by 64 array and a 1024 linear array

And Fairchild with startup Reticon

Peter JW Noble

Gene Weckler

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MOS-based charge-coupled devices (CCDs) shift charge one step at a time to a common output amplifier (1969 Bell Labs).
2009 Nobel Prize in Physics

"for the invention of an imaging semiconductor circuit – the CCD sensor"

CCD image sensor inventor: Michael F. Tompsett
US patent no. 4,085,456
National Medal of Technology and Innovation 2010
Cassini (1997) ISS has CCD cameras (wide angle and narrow angle)

Mass: 57.83 kg
Power (avg): 30.0 W
CCD: 1024x1024 pixels
NASA’s Administrator Daniel Goldin
“Faster, Better, Cheaper”

Need to Miniaturize Cameras
On Future Spacecraft to reduce mass, power, cost

• Electronics integration is well-worn path to miniaturization, and MOS-based image sensors predate CCDs (e.g. Peter Noble or Gene Weckler late 1960’s) including passive pixel and active pixel (3T) configurations.

• BUT MOS image quality is quite poor compared to CCDs due to temporal noise, fixed pattern noise and other artifacts.

• How to make a high performance image sensor in a mainstream CMOS process?
Active Pixels with Intra-Pixel Charge Transfer

- Complete charge transfer to suppress lag
- Correlated double-sampling to suppress kTC noise
- Double-delta sampling to suppress fixed pattern noise
- On-chip ADC, timing and control, etc.

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CMOS “Camera on a Chip”
2nd Generation Image Sensor
Read pixel signals out thru switches and wires

Row select logic chooses which row is selected for readout.

Timing and control logic controls the timing of the whole sensor.

Photodetector converts photons to electrons.
Amplifier converts electrons to voltage after intrapixel complete charge transfer.

Analog signal processor suppresses noise and further amplifies signal.
Analog-to-digital converters (ADC) convert signals from volts to bits (usually 10-12 bits resolution) in parallel.

Column multiplexer used to scan ADC outputs.

SoC functionality for color processing, compression, etc.

Digital Signal Proc.
Camera-on-a-Chip Enables Much Smaller Cameras

CMOS Active Pixel Sensor With Intra-Pixel Charge Transfer Camera-on-a-chip

Siimpel AF camera module 2007
Most of the JPL Team

Advanced Imager Technology Group, Jet Propulsion Laboratory, California Institute of Technology 1995
Back row: Roger Panicucci, Barmak Mansoorian, Craig Staller, Russell Gee, Peter Jones, John Koehler
Front row: Robert Nixon, Quisp Kim, Eric Fossum, Bedabrata Pain, Zhimin Zhou, Orly Yadid-Pecht
Commercialization
Entrenched industry moves slowly in adopting new technologies so in February 1995 we founded Photobit Corporation to commercialize the CMOS image sensor technology ourselves.

S. Kemeny, N. Doudoumopoulos, E. Fossum, R. Nixon
1995-2001 Photobit grows to about 135 persons
• Self funded with custom-design contracts from private industry
• Important support from SBIR programs (NASA/DoD)
• Later, investment from strategic business partners to develop catalog products
• Over 100 new patent applications filed
The Photobit Team Circa 2000
Nov. 2001 – Photobit acquired by Micron Technology and license reverts back to Caltech

Meanwhile, by 2001 there were dozens of competitors emerging in the CMOS image sensor business due in part to the earlier efforts to promote the transfer the technology.

Examples: Toshiba, ST Micro, Omnivision

Micron becomes #1 in CMOS image sensor sales and market share

Later, came Sony and Samsung (now #1, #2 in worldwide market)

Micron spins out Aptina
Aptina acquired by ON Semi, currently #4
The Technology Develops a Life of its Own

- Today, over 2 billion cameras are manufactured each year that use the CMOS image sensor technology we invented at JPL, or more than 60 cameras per second, 24/7/52
- Semiconductor sales of CMOS image sensors will be $10B/yr by 2016.
- Thousands of engineers working on this.
- Caltech has successfully enforced its patents against all the major players.
- NASA is now just adopting the technology for use in space.
New Technology Invariably Brings New Social Issues

- Selfies and Instant Communications
- Rapid Social Change (Arab Spring)
- Body Cameras
- Drone Cameras
- Visual overload (e.g. Japanese Tsunami)
- Security v. Privacy
- Inappropriate use

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Some Science and Technology
Diffraction Limit

LENS

Airy Disk Diameter

\[ D = 2.44 \lambda F\# \]

Cheap Lens Resolution

(30 lp/mm)

High Performance Lens Resolution

(120 lp/mm)

Size (microns)

Wavelength (nm)

F/2.8

F/11

B G R
Photon Shot Noise

- Photon emission is a Poisson process. Stream of photons is NOT regularly spaced.

- Leads to variability when trying to determine average photon arrival rate. Gets better with longer measurement (more photons).
Photon Shot Noise in Pictures
Microlenses

- Main camera lens brings image to microlenses
- Microlens funnels photons to active detector area.

Light Rays

Microlens layer
Color filters
Metal wiring
Opaque layer
Photodetector
Silicon substrate
• Each pixel gets covered by a colored filter
  – We use red, green, blue (RGB) CFA - best match for RGB displays
  – Pixel colors arranged in “Bayer” pattern G R B G (assumes UV and NIR filters)
Photons to Electrons

Covalently bonded silicon

Higher energy blue photon gets absorbed sooner

Pinned photodiode

N. Teranishi et al. 1982 for ILT CCD
CMOS Pinned Photodiode Pixel

"4T architecture"

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Shared Readout Architecture

“1.35T architecture”

Sony 1.4 um BSI pixel
Backside Illumination (BSI)

Sony 1.4 um BSI pixel
Deep Trench Isolation for Crosstalk
Stacked CMOS BSI

Quanta Image Sensor
L-R: Song Chen, Saleh Masoodian, Rachel Zizza, Donald Hondongwa, Dakota Starkey, Eric Fossum, Jiaju Ma, Leo Anzagira
- Additional Members -
- Arun Rao
- Yue Song
- Prof. Kofi Odame
- Mike Guidash (Rambus)
- Jay Endsley (Rambus)
- Prof. Yue Lu (Harvard)
- Prof. Atsushi Hamasaki (Hiroshima)
- Mr. Ryohei Funatsu (NHK)

- QIS work supported, in large part, by -
  - Rambus Inc.
Original goal for QIS was to take advantage of shrinking pixel size and make a very tiny, specialized pixel ("jot") which could sense a single photoelectron.

Jots would be readout by scanning at a high frame rate to avoid likelihood of multiple hits in the same jot and loss of accurate counting.

Image pixels could be created by combining jot data over a local spatial and temporal region using image processing.

The first proposed algorithm was the "digital film sensor" using a "grain" and "digital development" construct.
Simplest

\[ \sum_{X'Y't'} j(X,Y,t) \]

16x16x16 “cubicle”

0 \leq S \leq 4096

R. Zizza, Jots to Pixels: Image Formation Options for the Quanta Image Sensor, (Dartmouth, 2015)
QIS Core Architecture

- JOT ARRAY
- ROW SCAN
- COLUMN SENSE AMPLIFIERS

TIMING AND ROW DRIVERS
Figure of Merit: Flux Capacity $\phi_w$

At the flux capacity, there is an average of one photoelectron per jot

$$\phi_w = j f_r / \sigma \bar{\gamma}$$

- $j = $ jot density (per cm$^2$)
- $f_r = $ field readout rate (per sec)
- $\sigma = $ shutter duty cycle
- $\bar{\gamma} = $ average quantum efficiency

• At 500nm jot pitch, 1000fps, 100% duty cycle and 35% QE, $\phi_w \approx 10^{12} / cm^2 s$

• Corresponds to ~100lux (555nm, F/2.8, RT=80%)

➤ Drives high jot density and field readout rate so can handle normal lighting conditions
➤ And improve SNR per sq. cm of sensor area.
Multi-bit Jot Increases Flux Capacity

At the flux capacity, there is an average of \( 2^n - 1 \) photoelectrons per \( n \)-bit jot

\[
\phi_{wn} = j f_r (2^n - 1) / \sigma \bar{y}
\]

\( \Rightarrow \)

- Can increase flux capacity at same jot density and field readout rate
- Or, relax field readout rate and/or jot density for same flux capacity

Little impact on detector and storage well. Little impact on FD CG or voltage swing (e.g. \( 1\text{mV/e} \) -> \( 31\text{mV swing for 5b jot} \).
Photon and photoelectron arrival rate described by Poisson process

Define *quanta exposure* $H = \phi \tau$  
$H = 1$ means expect 1 arrival on average.

Probability of $k$ arrivals

$$P[k] = \frac{e^{-H} H^k}{k!}$$

Monte Carlo

For jot, only two states of interest

- $P[0] = e^{-H}$
- $P[k > 0] = 1 - P[0] = 1 - e^{-H}$

For ensemble of $M$ jots, the expected number of 1’s:

$$M_1 = M \cdot P[k > 0]$$
Bit Density

\[ D \triangleq \frac{M_1}{M} = 1 - e^{-H} \]

Can determine \( H \) from measured \( D \)

\[ H = \ln \left[ \frac{1}{1 - D} \right] \]
QIS implementation requires Devices, Circuits, and System

Strawman numbers

- <500 nm jot pitch
- Gigajot QIS (10^9 jots)
- 1000 fps
- 1 Tb/s data rate
- 1 Watt or less (<1pJ/b)
23mW 1000fps
1 Mpix binary image sensor

- XFAB 0.18um 1.8V
- 1376(H) x 768(V) 3.6um 3T CDS
- 119uV/e-, 2e-rms, ~5.2e- threshold
- 768KSa/s
- 1 Gb/s data rate
- Whole chip incl. pads 20mW
- ADCs 2.6mW
- Energy 2.5pJ/b
Poisson Distribution (scaled)

\[ P[k] = \frac{e^{-H} H^k}{k!}, \quad k = 0, 1, 2, 3 \ldots \]
Broadened by 0.12e- rms read noise

Model
Broadened by 0.25e- rms read noise
Probability Distribution for Various Levels of Read Noise

Model
Single-bit QIS

Poisson Distribution
- 0.12e- rms
- 0.15e- rms
- 0.25e- rms
- 0.35e- rms
- 1.0e- rms

Voltage/CG = Electron Number

Probability Density

- “0”
- “1”
BER vs. Read Noise

Single-Bit QIS BER

- Total BER vs. Read Noise (e- rms)
- Curves for different values of H: H=0.1, H=0.2, H=0.5, H=1, H=2, H=5
- Key points: 1/20, 1/2,500

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Multi-bit QIS (e.g. 2-bit)

Poisson Distribution
- 0.12e- rms
- 0.15e- rms
- 0.25e- rms
- 0.35e- rms
- 1.0e- rms

Voltage/C0 = Electron Number

“00”  “01”  “10”  “11”
Single Bit v. Multi-bit

**Single Bit**
- Each jot produces 1 bit
- 1 bit ADC
- For same flux capacity, need higher frame rate readout
- Conceptual simplicity
- Easier on chip digital electronics

**Multi-bit**
- Each jot produces n bits
- n-bit ADC
- For same flux capacity, lower relative frame rate $\frac{1}{2^{(n-1)}}$
- Like current CMOS APS but low FW capacity and high conversion gain

*S, Chen, A. Ceballos, E.R. Fossum, 2013 IISW*
Jot Device Considerations

General targets:
- 200 nm device in 22 nm process node (“10L”)
- 0.15e- rms read noise or less
- High conversion gain > 1 mV/e- (per photoelectron)
- Low active pixel transistor noise <150 uV rms
- Small storage well capacity ~1-100 e-
- Complete reset for low noise
- Low dark current ~ 1 e-/s
- Not too difficult to fabricate in CIS line

Candidate devices
- Single photon avalanche detector (SPAD)
- Single electron FET
- Bipolar jot
- **Pump gate jot**
- JFET jot
Pump-Gate Jot

Fabricated in TSMC 65nm BSI CIS

1.4um pitch

Ma and Fossum
2014 IEDM, 2015 JEDS, 2015 EDL
Experimental Data
Photon-Counting Histograms

- 200k reads of same jot, ~0.28e- rms read noise, 120uV rms, 430uV/e-, ~60DN/e-
  Room Temperature, No Avalanche, Single CDS readout
Ma, Starkey, Rao, Odame and Fossum, submitted to IEEE JEDS Aug 2015

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Ma, Starkey, Rao, Odame and Fossum, submitted to IEEE JEDS Aug 2015
Experimental Data
Photon-Counting Histograms

200k reads of same jot, ~0.22e- rms read noise, 93uV rms, 423uV/e-, ~60DN/e-
Room Temperature, No Avalanche, Single CDS readout

“golden jot”
Mean exposure ~9e-

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