Quanta Image Sensor:
Possible paradigm shift for the future

Eric R. Fossum
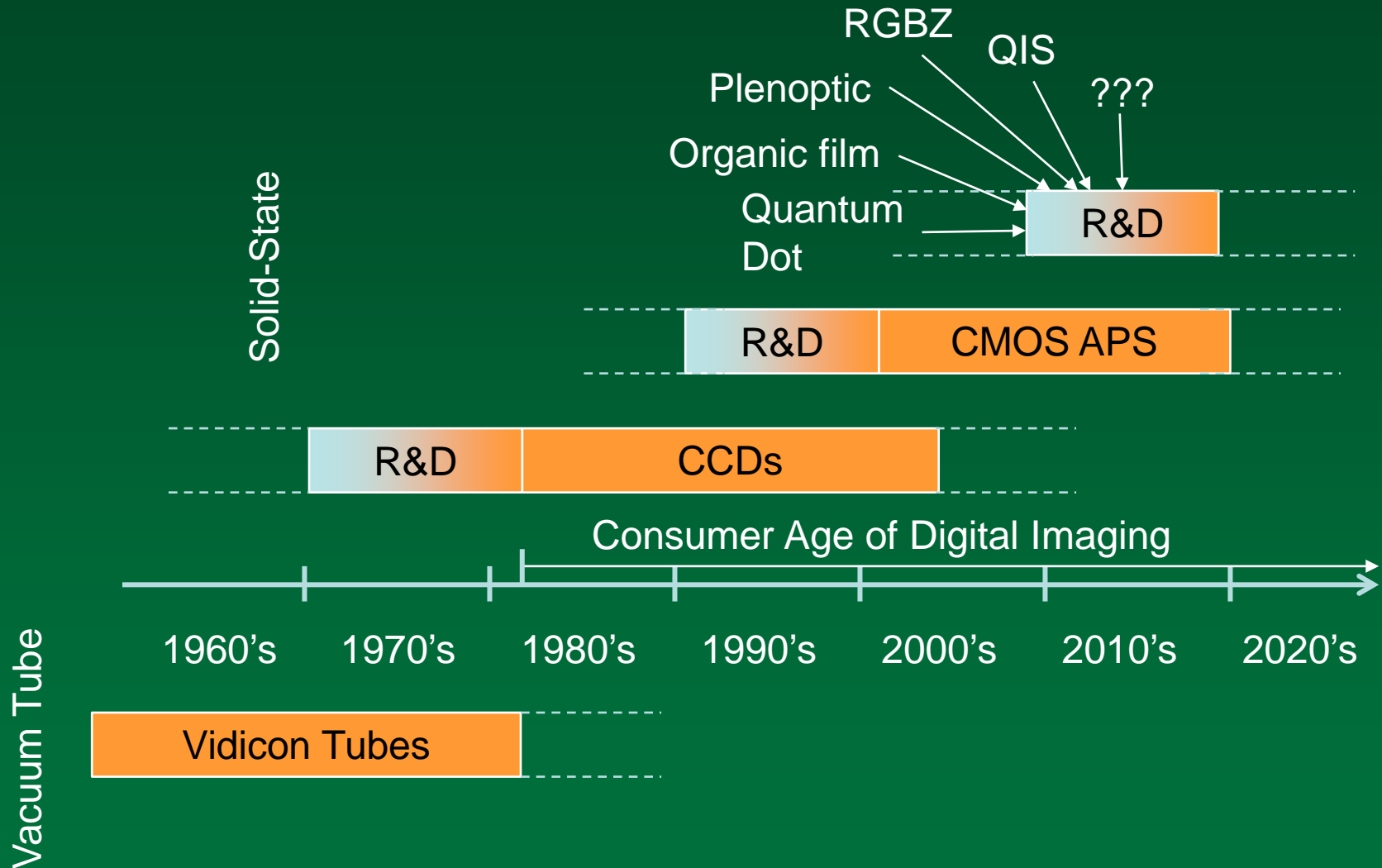
March 22, 2012

"Grand Keynote", IntertechPira Image Sensors 2012

London, England, UK

Technology Timeline

THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

Solid-State

RGBZ
QIS
Plenoptic
???
Organic film
Quantum Dot

R&D

R&D CMOS APS

R&D CCDs

Consumer Age of Digital Imaging

1960's 1970's 1980's 1990's 2000's 2010's 2020's

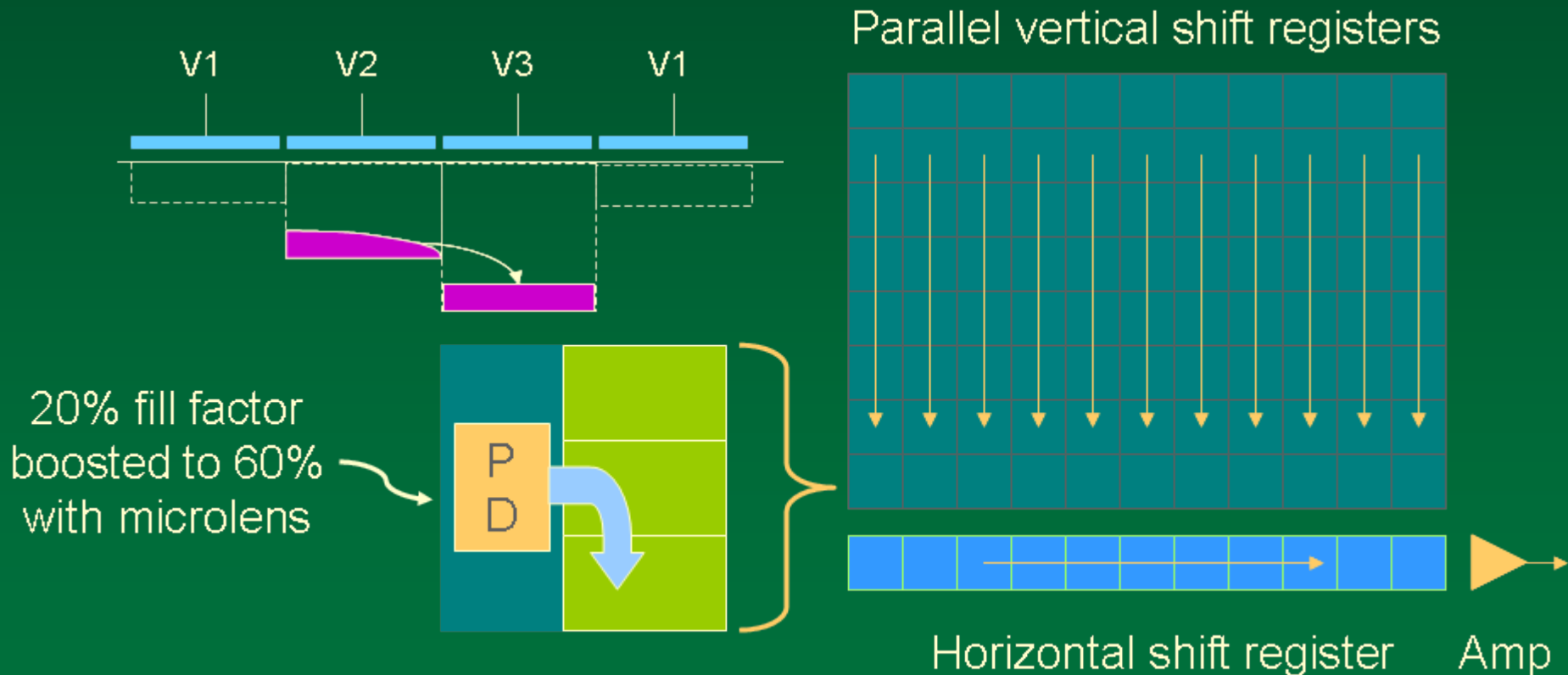**Vacuum Tube**

Vidicon Tubes

Charge-Coupled Device 1st Generation Image Sensor

- MOS-based charge-coupled devices (CCDs) shift charge one step at a time to a common output amplifier

V1　V2　V3　V1

20% fill factor boosted to 60% with microlens

P D

Parallel vertical shift registers

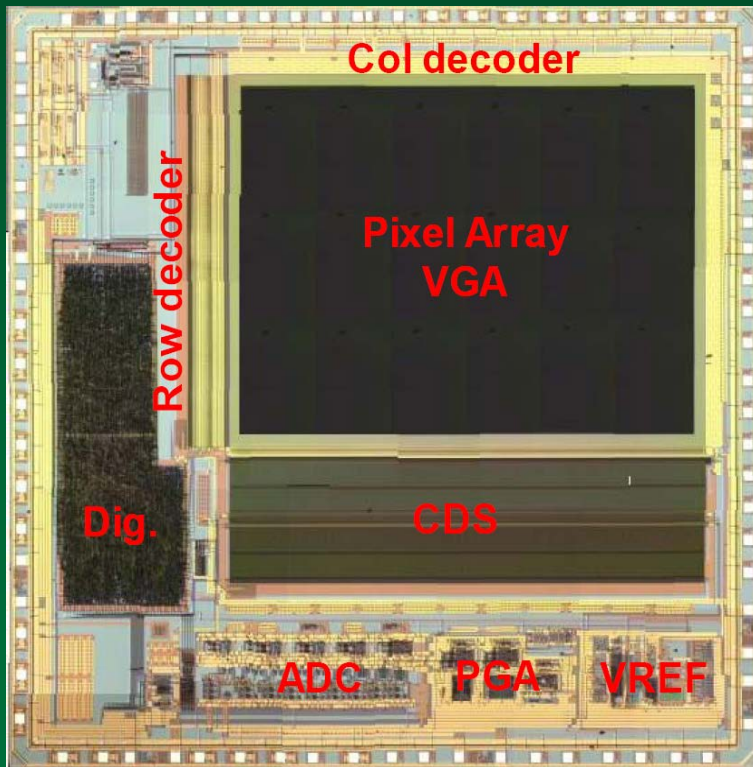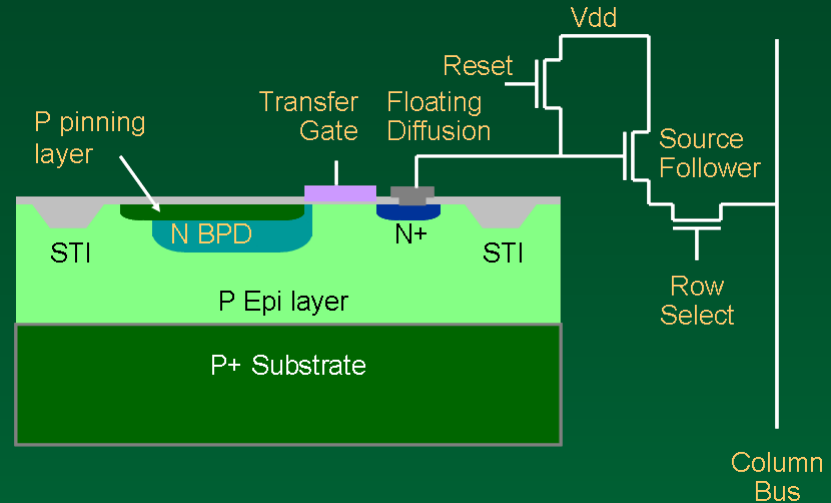Horizontal shift register　　Amp

CCD Limitations

- Requires high charge transfer efficiency
  - Special fabrication process adds cost
  - Larger voltage swings, different voltage levels
- Difficult to integrate on-chip timing, control, drive and signal chain electronics
  - Process integration increases cost, reduces yield
  - Large capacitances require high current levels
- Requires timing generator chip, driver chips, signal processor, ADC and interface chips
- System power in 0.5-2 Watt range
- Architecture yields serial access to image data
- Limited frame rates

CMOS Active Pixel Sensor
2nd Generation Image Sensor

Pain et al.
2007 IISW

Col decoder

Row decoder

Pixel Array
VGA

CDS

Dig.

ADC   PGA   VREF

Vdd

Reset

Transfer Gate

Floating Diffusion

P pinning layer

Source Follower

STI   N BPD   N+   STI

P Epi layer

P+ Substrate

Row Select

Column Bus

Camera on a Chip

- Active pixel array
- Analog signal chain
- Analog-to-Digital Conv.
- VLSI Digital logic
  - I/O interface
  - Timing and control
  - Exposure control
  - Color processing
  - Ancillary circuits

-5-

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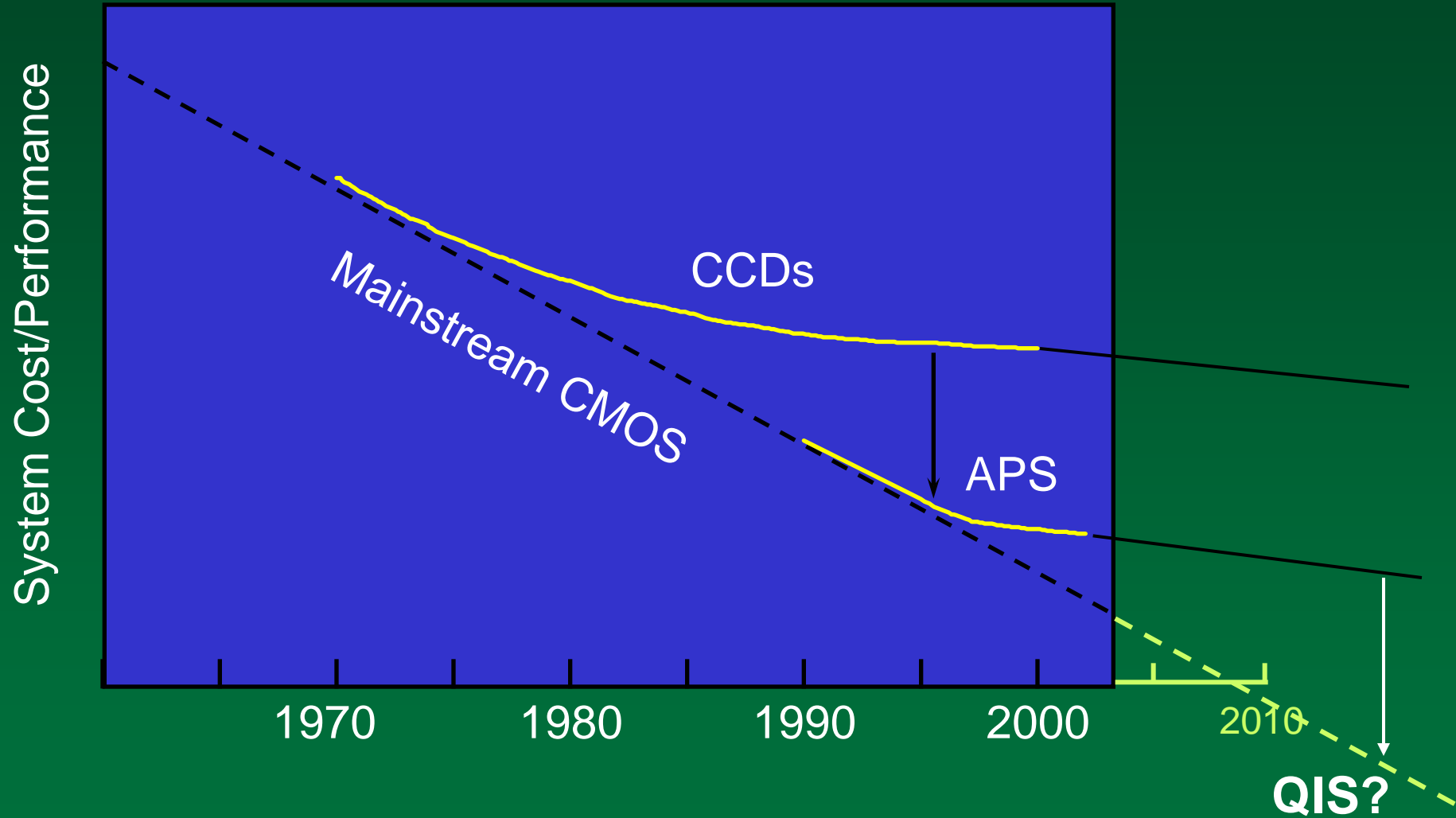ENGINEERING
AT DARTMOUTH

State of the Art

- Widely adopted in 2012

- ~2,000 million units/yr

- ~4,000 cameras/min 24/7

- Camera phones, web cams, DSLRs, medical, automotive, scientific, etc.

- Pixel sizes 1.1-1.4 um

- Arrays 8-16 Mpixels

- Image quality is quite satisfactory

Future Mainstream CMOS Characteristics

- Use of nanometer-scale nodes
  - e.g. 22 –> 14 nm
- Lower operating voltages
  - 0.8 –> 0.4 volts
- Use of materials other than silicon
  - e.g. such as graphene, SiGe, or InGaAs on silicon
- Use of 3D gates structures
  - Tri-gate or finFET

All of these trends are problematic for CMOS APS

- In 1994 we thought it was a great challenge to make a pinned photodiode operate with a 5V swing.
  - What about 0.5 volt swing?
- Noise reduction has, in part, been accomplished with higher conversion gain, but this requires larger rail voltages to achieve the same full well.
  - 10k e- full well at 100 uV/e- requires 1 volt swing
- Analog signal chain much easier at 1 volt rail-to-rail, or higher.

Charge storage in buried or pinned photodiode

Fig.2. Band diagram of pinned photodiode
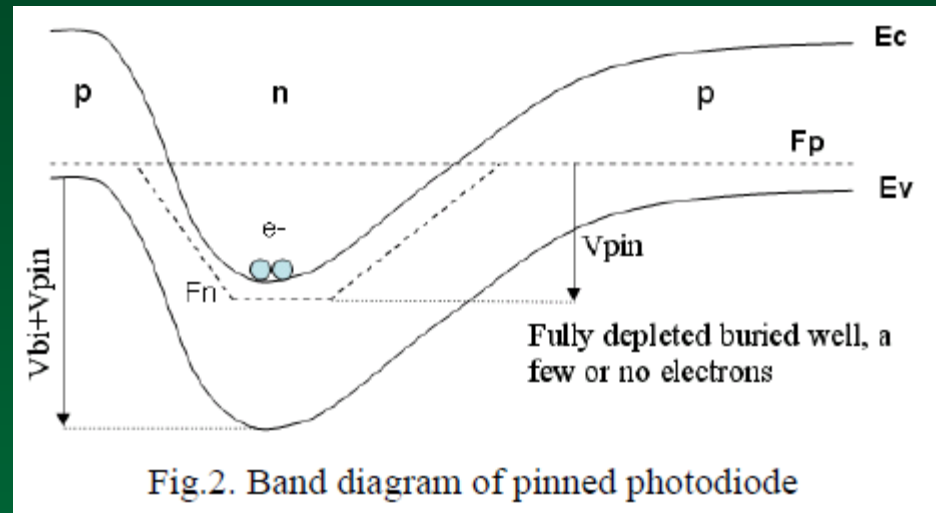
Krymski, 2005 IISW

- No Si-SiO$_2$ interfaces, low trapping and generation
- All silicon, well gettered, few defects
- Diffusion-limited dark current
- Complete charge transfer for readout
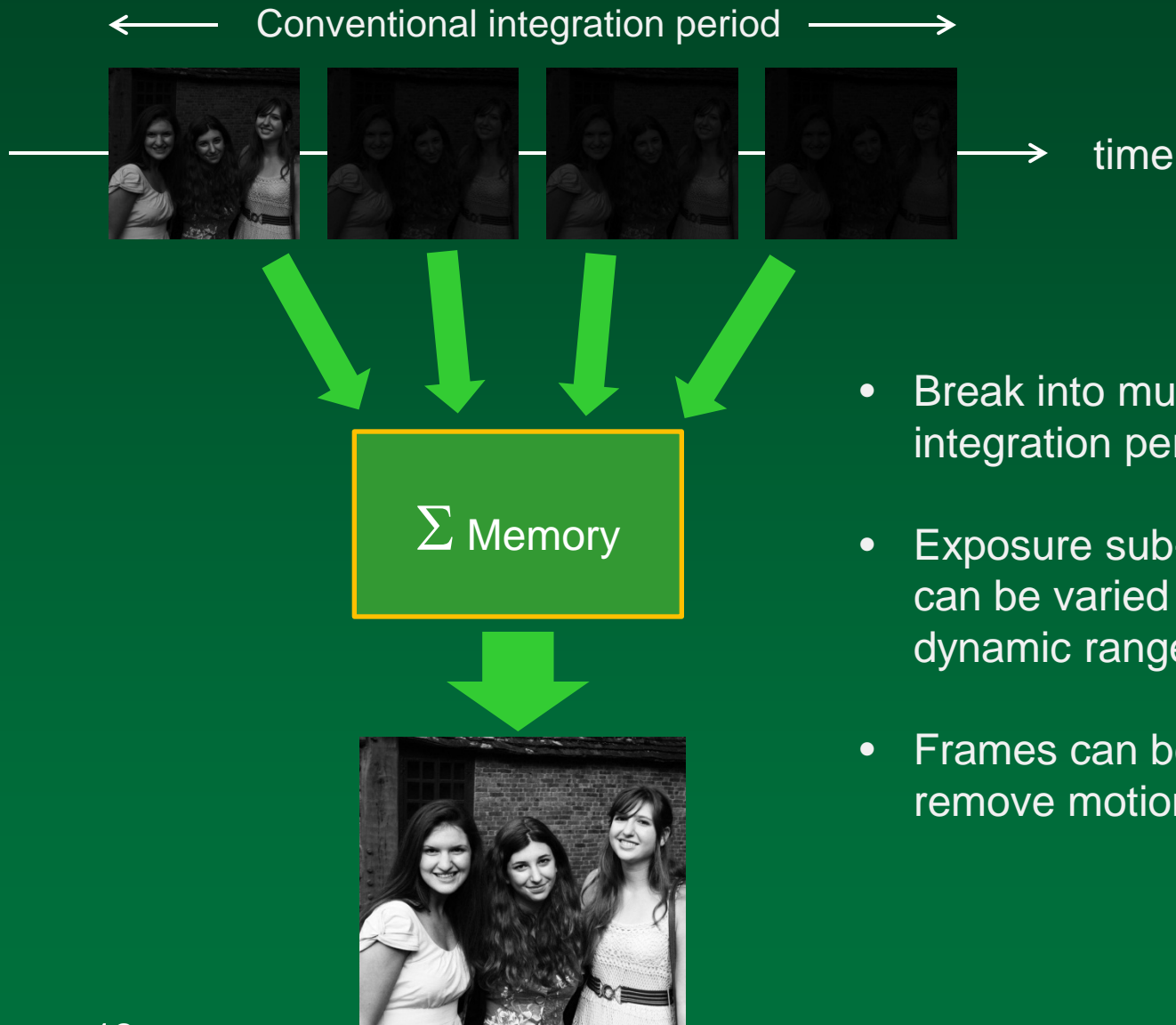- "Large" structure, must store full well signal.

Digital Integration Sensor

- Can relieve issues with pinned photodiode capacity, readout electronics full well capacity, and improve dynamic range.

- Deliberately make full well capacity much smaller in pinned photodiode (easier design and process)

- Use higher conversion gain to improve read noise (reduced FD area and capacitance)

- Add successive fast frames in digital memory.

See Hynecek US Patent No. 7,825,971 and Patent Applications by Fossum 2011
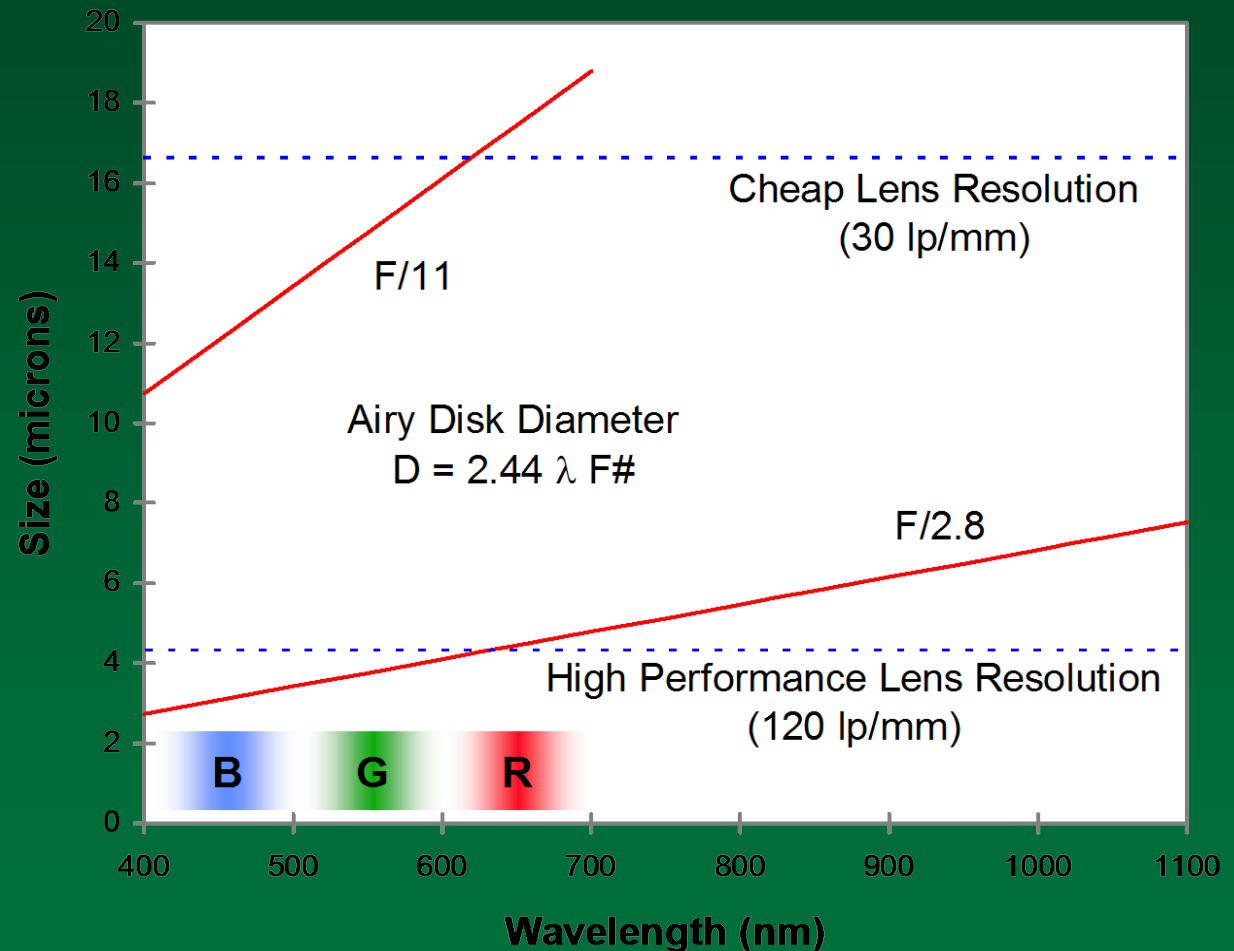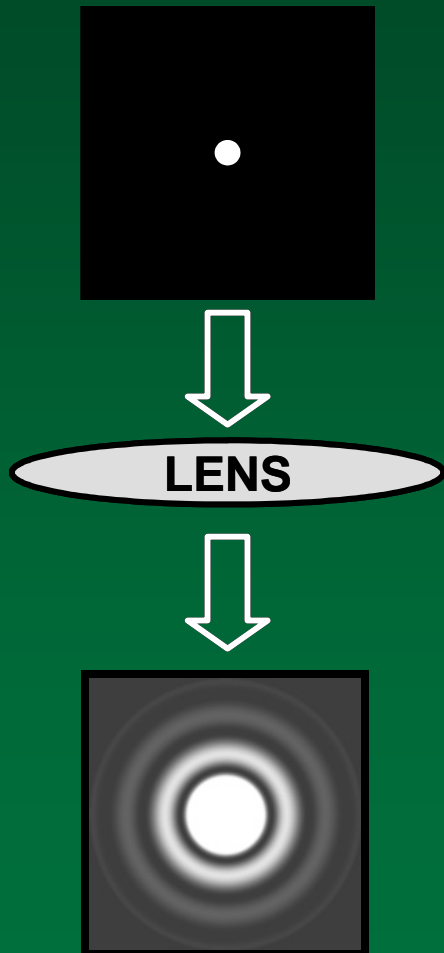
Digital Integration Sensor (DIS)

Conventional integration period

time

Σ Memory

- Break into multiple sub-integration periods

- Exposure sub-integration times can be varied to increase dynamic range

- Frames can be shifted to remove motion blur

- Relentless drive to lower sensor costs

- And continued drive to higher resolution

- Pixel sizes at 1.1 um with 0.9 um coming soon.

- Higher speed readout

- Higher dynamic range

- Have relied on baseline CMOS technology scaling to help with pixel scaling.

- Have not really had to deal with sub-diffraction limit pixels in a serious way

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LENS

Cheap Lens Resolution
(30 lp/mm)

F/11

Airy Disk Diameter
D = 2.44 λ F#

F/2.8

High Performance Lens Resolution
(120 lp/mm)

B G R

Size (microns)

Wavelength (nm)

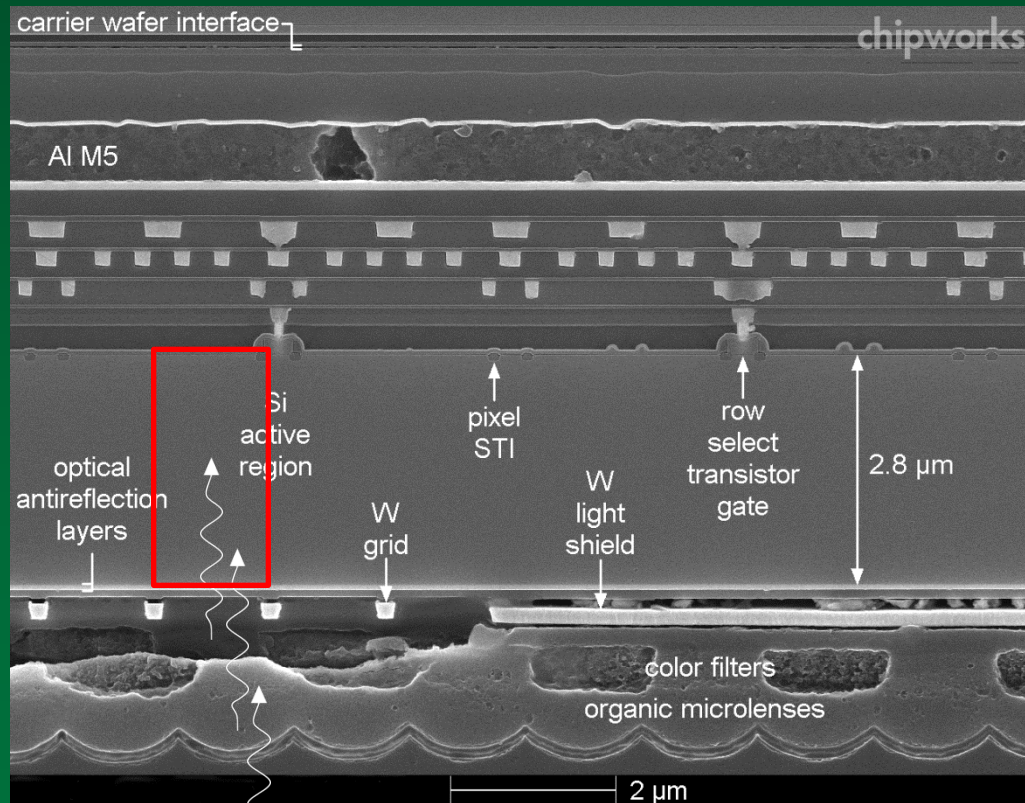# Sub-Diffraction Limit Pixels

0.9 um pixel pitch

- Marginal return on shrink for real resolution improvement
- Sort of a spatial and color oversampling
- Anti-aliasing filter not needed

- Some real limit on how small is practical according to current pixel paradigm

- Could possibly remove diffraction effect by ISP but would probably reduce SNR
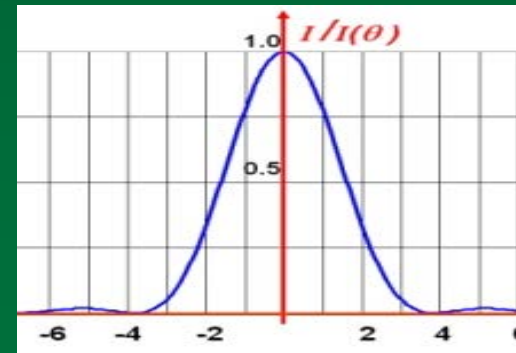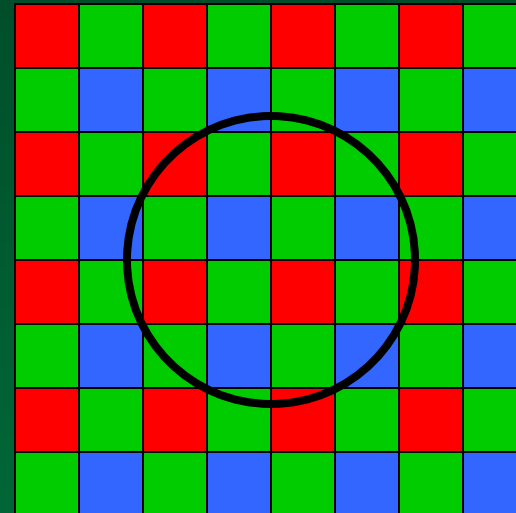
Absorption Length Scaling

- Absorption length $1/\alpha$ does not scale in any easy way, and can cause cross talk and loss of resolution.

carrier wafer interface

chipworks

Al M5

Si active region

pixel STI

row select transistor gate

2.8 µm

optical antireflection layers

W grid

W light shield

color filters
organic microlenses

2 µm

-16- Light

Sony 8MP BSI sensor in iPhone4S
Courtesy R. Fontaine, Chipworks

- Can consider other materials like a-Si, organic films and quantum dots but their use has noise and mfg. issues
- Silicon is very special and well developed.

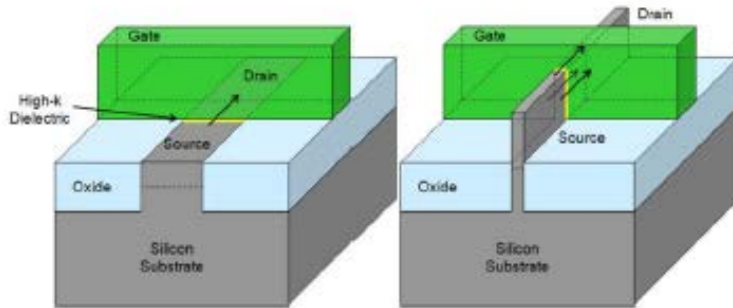175 nm

$\sim 1/\alpha_{RED}$

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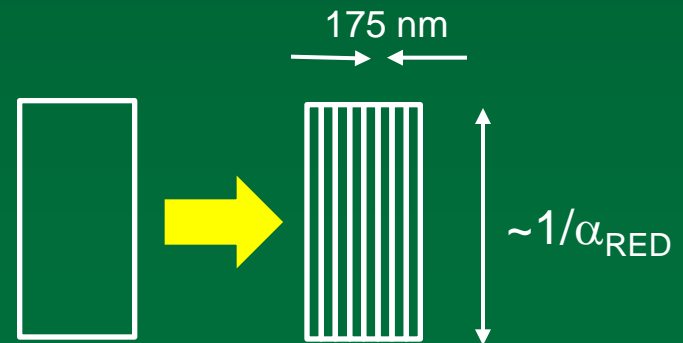
Figure 8: Traditional planar transistor structure (left) compared to 3-D Tri-Gate transistor structure (right)
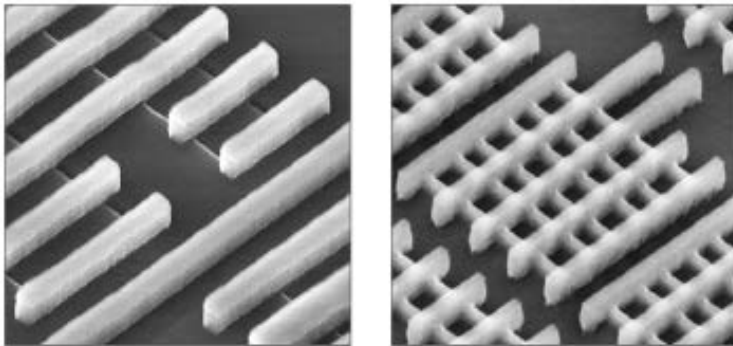

Figure 9: SEM image of 32 nm planar transistors (left) compared to 22 nm Tri-Gate transistors (right)
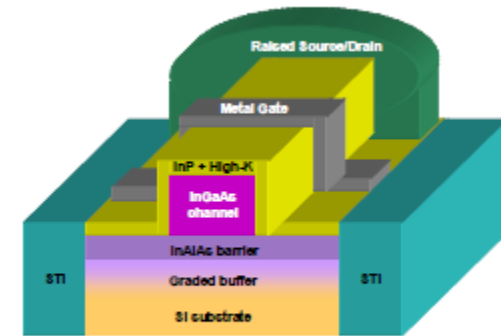

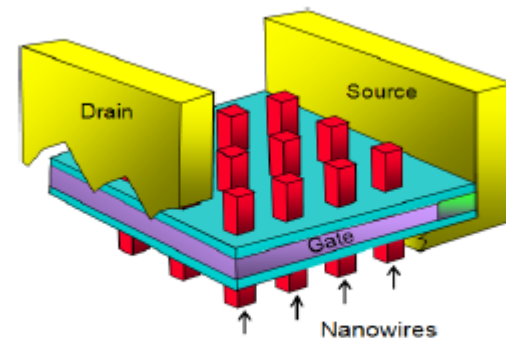Figure 13: Multi-gate InGaAs QWFET structure
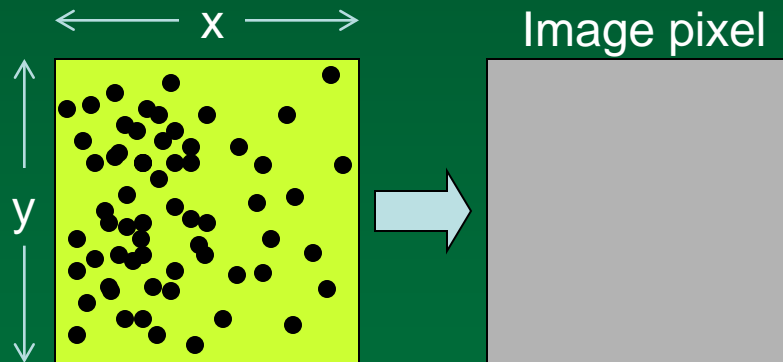

Figure 15: Nanowire FET structure with vertically oriented channels
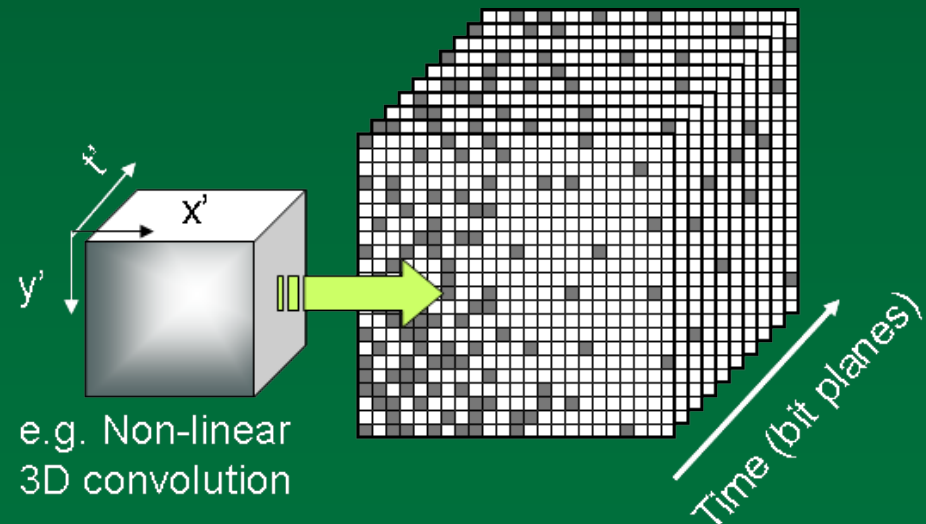
M. Bohr, 2011 IEDM

Current paradigm:

- We collect photons for a predetermined amount of time in a silicon "rainbucket" determined by physical size and capacity of silicon pixel.

New paradigm:

- Let's count each photogenerated carrier and record time and location, creating binary bit planes for each time slice, and then digitally form image by digital convolution over X,Y, t.

x

y

Image pixel

t'

x'

y'

e.g. Non-linear 3D convolution

Time (bit planes)

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- A Quanta Image Sensor (QIS) is an array of specialized photon-counting pixels called jots.

- A QIS might contain 1-100 Gjots.

- A QIS is read out 250-1000 times per second.

- A QIS generates about 0.25- 100 Tbits/sec data rate.

- The Tbit/sec data can be processed on-chip and off-chip to form an image.

Core QIS Architecture

TIMING AND ROW DRIVERS

JOT ARRAY

ROW SCAN

COLUMN SENSE AMPLIFIERS
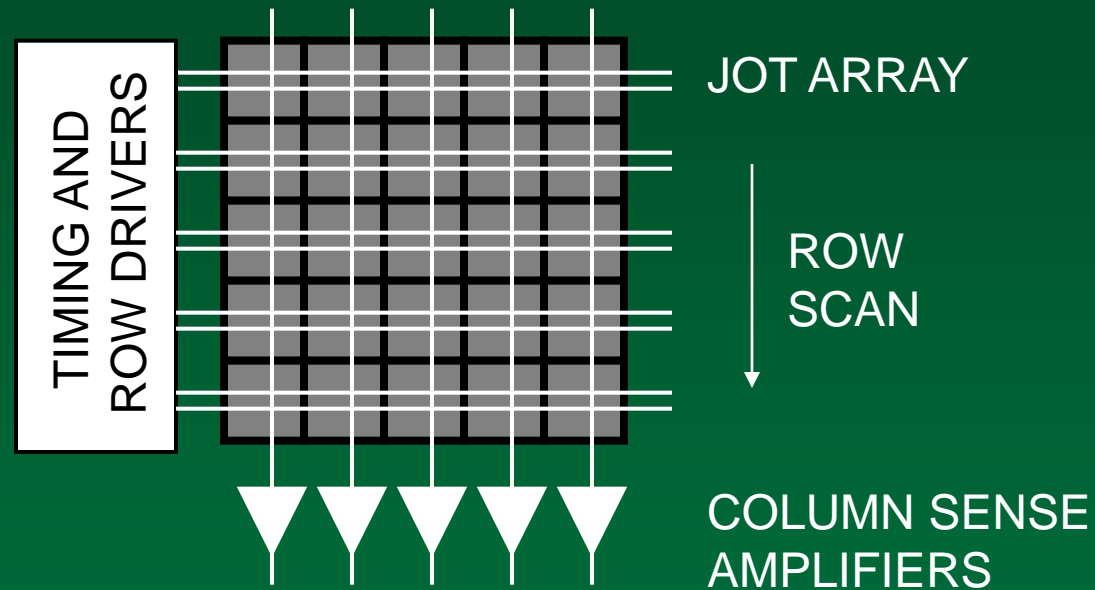
• Shift successive frames based on known scan direction, image-based motion flow or guide star

Track and Sum

- Solid-State Photon Counting in Visible (Low noise, big pixels)
  - Image intensified image sensors (CCD and CMOS APS)
  - Electron multiplying CCDs (internal avalanche)
  - Single photon avalanche detectors (SPADs)
  - Nano-multiplication-region avalanche photodiode (NAPD)
  - Amplified pixels with sub-electron read noise.
- Binary Pixels using DRAM (Threshold detectors, small pixels)
  - Micron "eye"
  - Gigavision camera
- Digital Pixels (Analog pixel, digitize and count in or near pixel)
  - Digital pixel sensor (DPS)
  - NHK Digital image sensor
- Image Stabilization and HDR
  - "Anti-shake" by adding high-speed frames offset from one another
  - High dynamic range by merging 2-3 differently exposed frames
  - "Lucky" imaging in astronomy
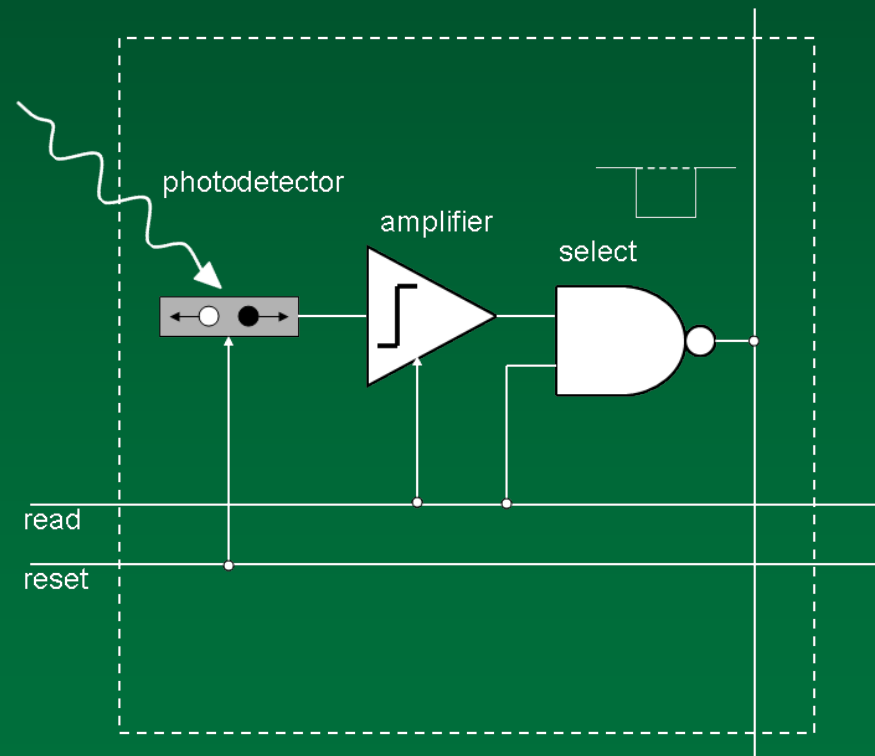
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- A jot is an nano-scale active pixel with binary output sensitive to a single photocarrier
- Takes many jots (space and/or time) to make an image pixel.

Jot Functionality
1. Photodetector
2. High gain
3. Select/drive
4. Reset

Could be merged to one or two devices per jot

photodetector

amplifier

select

read

reset

Functional illustration only

There are several avenues for jot implementation.

1. Brute force scale-down of CMOS active pixel sensor. Read noise must be reduced. Achieving required dimensions challenging.

2. Modify a SPAD or NAPD device for QIS application.

3. Single-electron field effect transistor (SEFET). One electron causes enough current change to be detected by column sense amplifiers.

4. Stacked device (e.g. using Si_xGe_{1-x})

5. New device to-be-invented based on quantum dot film or other nanoscale device.

Front side of wafer
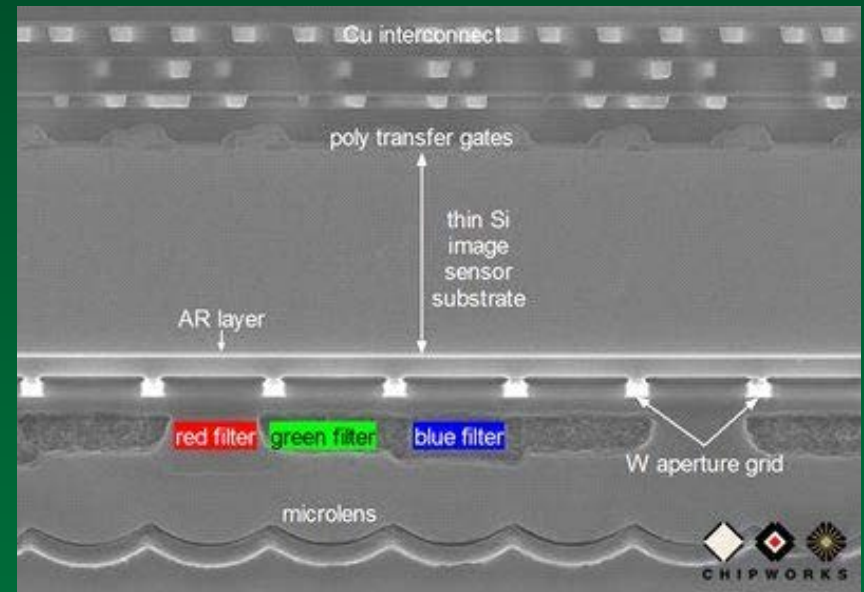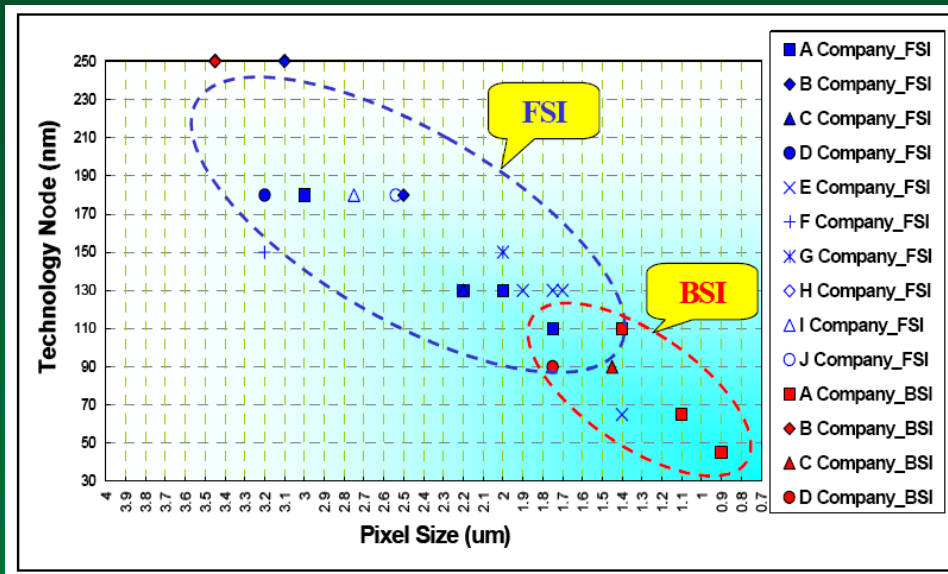
Pixel Trend From TSMC

Example from Sony

Light

- Requires shrink from 900 nm to 200-100 nm scale. About 20-80 x decrease in pixel area.

- Requires increase in conversion gain of about 200x. (50 uV/e- -> 10 mV/e-)

- Requires decrease in input-referred read noise of about 20x from 3 e- rms -> 0.15 e-

- Requires decrease in full well from 3000 e- to 1-10 e- (this part is easy).

* Note that future sub-electron read noise in CMOS APS can lead to photon counting, which at low counts is like a multi-level jot, albeit not a pure jot.

A 32x32 SPAD Pixel Array with Nanosecond Gating and Analog Readout

Lucio Pancheri, Nicola Massari, Fausto Borghetti and David Stoppa

Fondazione Bruno Kessler, Via Sommarive, 18, 38123 Trento, Italy

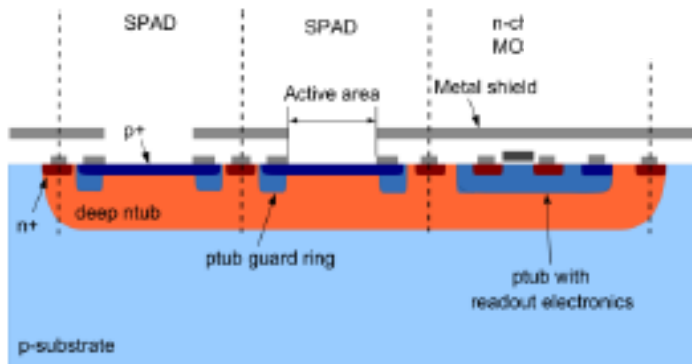phone: +39 0461 314147, fax: +39 0461 314591, e-mail: pancheri@fbk.eu
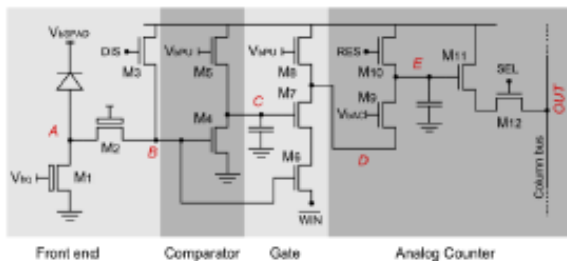

Figure 2. Pixel-array cross section.

Figure 1. Pixel schematic diagram.
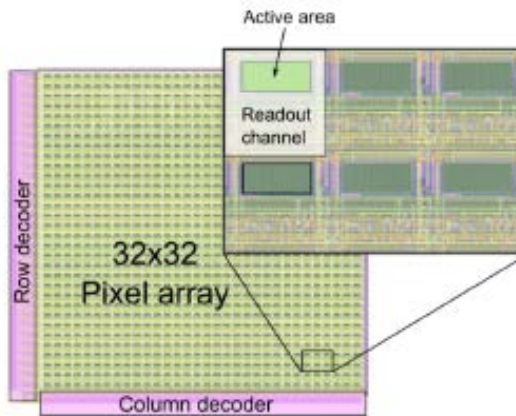

Figure 5. Sensor and pixel layout.
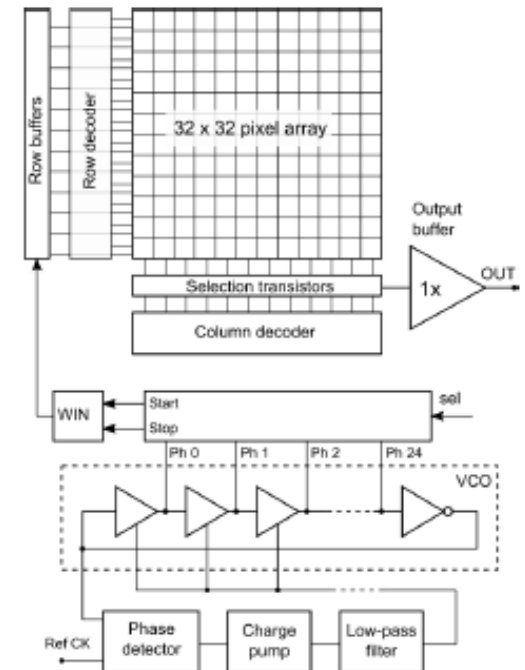
Figure 4. Sensor architecture.

- SPAD size must be reduced from ~5000 nm pitch to 200-100 nm (about 600-2500x change in pixel area).

- Can eliminate SPAD timer circuitry.

- Replace continuous time circuitry with read/reset select-activated circuitry.

- Increase SPAD count from 32x32 (1024 elements) more than one million fold.

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Samsung

Status:
- TCAD model only
- Shows about 5-10 mV/e- signal
- More work required

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Fairchild Imaging sCMOS	www.scmos.com
Sensor format	5.5 megapixels (2560(h) x 2160(v))
Read noise	< 2 e- rms @ 30 frames/s; < 3 e- rms @ 100 frames/s
Maximum frame rate	100 frames/s
Pixel size	6.5 μm
Dynamic range	> 16,000:1 (@ 30 frames/s)
QEmax	60% (with excellent red/NIR response)
Read out modes	Rolling and Global shutter (user selectable)

Table summarizing properties of sCMOS from Fairchild Imaging

- Total equiv. data rate $Q = N_{pix} \times N_{fw} \times F$ where
- N_{pix} = number of pixels, N_{fw} = full well, and F=frame rate
- For sCMOS, $N_{pix} = 5.5 \times 10^6$, $N_{fw} = 2 \times 16,000$, F=30
- Equiv data rate Q = 5.3 Tb/s
- (We ignore the chance that a jot captures more than one carrier which is not a good assumption near saturation.)

Pixels to Jots

1 pixel   4,225 jots
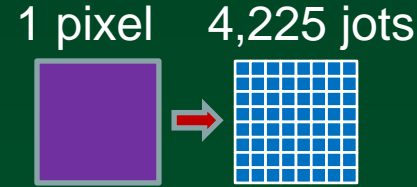
- 6500 nm pixel pitch
- Say, 100 nm jot pitch, or 65x65 jots per pixel
- At saturation, this is 4,225 electrons
- For N_{fw} of 31,700, need 8 of these = 33,800
- Jot field rate is 8x pixel frame rate = 240 fps.
- Pixels 2,560H x 2,160V = 5.5 Mpixels
  x 65H x 65V
- Jots 166,400H x 140,400V = 23.4 Gjots
- 23.4 Gjots x 8 x 30fps = 5.6 Tb/s
- Column scan rate (down column) is
  140,400V x 240 fps = 33.7 MHz

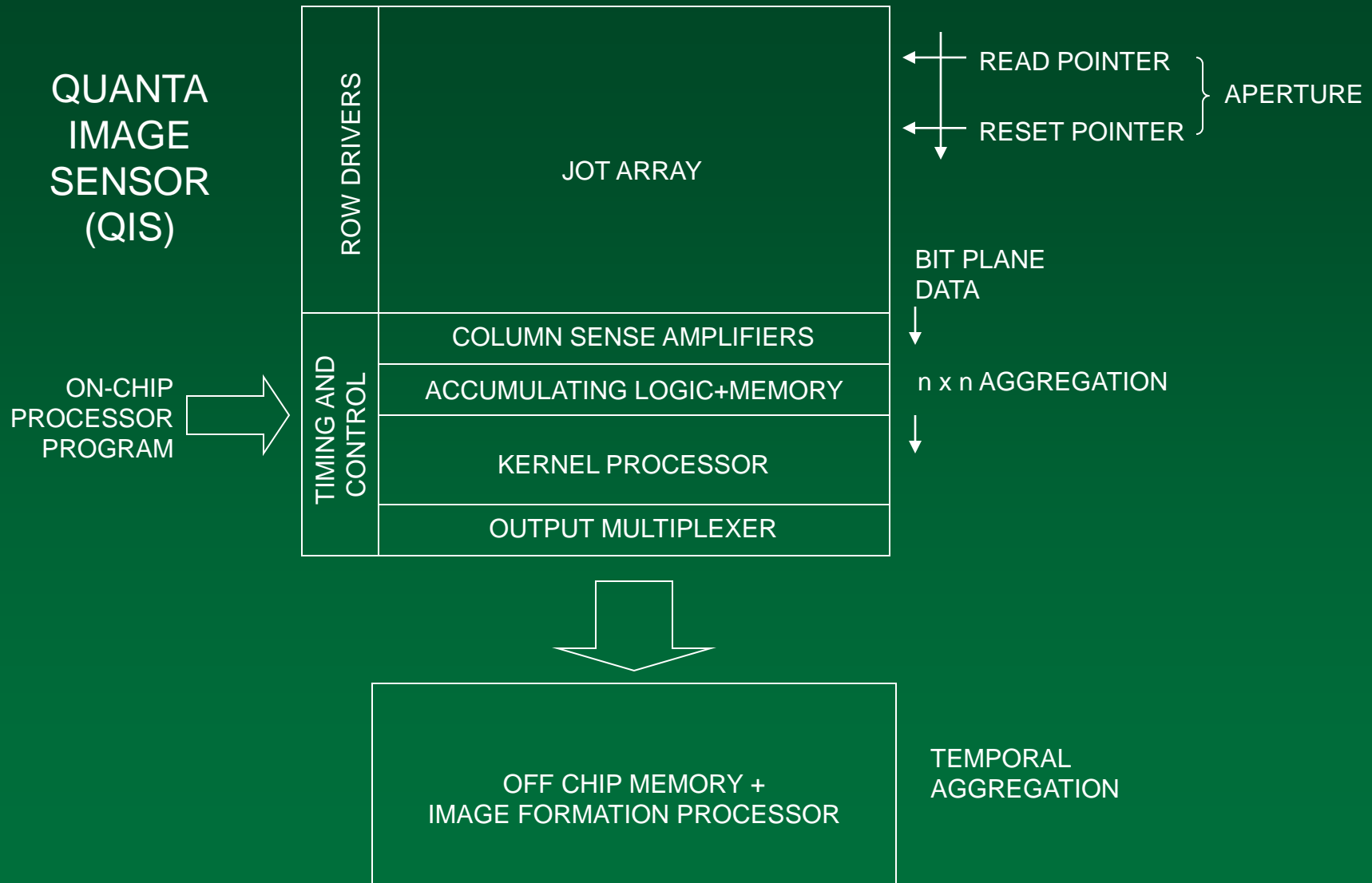| Sensor	sCMOS	Aptina 8M	sCMOS	Aptina 8M
Pixel Pitch (nm)	6500	1400	6500	1400
Pixels H	2560	3264	2560	3264
Pixels V	2160	2448	2160	2448
Total (Mpix)	5.5	8.0	5.5	8.0
Full Well (e-)	31700	3000	31700	3000
Frame Rate (Hz)	30	15	30	15
Te-/sec	5.3	0.4	5.3	0.4
Jot Pitch (nm)	100	100	200	200
Jots/Pixel	4225	196	1056	49
Jots H	166400	45696	83200	22848
Jots V	140400	34272	70200	17136
Total (Gjot)	23.4	1.6	5.8	0.4
e-/jot/frame	7.5	15.3	30.0	61.2
Bit plane readout (Hz)	225.1	229.6	900.4	918.4
Column scan rate (MHz)	31.6	7.9	63.2	15.7
Total jot rate (Tb/sec)	5.3	0.4	5.3	0.4
After KP (Gb/s)	1.2	1.8	5.0	7.3

- A fun challenge to consider getting 5+ Tb/s data rate off chip.

- Can put on-chip kernel processor to reduce raw data.
  - Example 1: Aggregate bits over some window
    - Horizontal and vertical binning of bits in i x j neighborhood.
    - Easy for binary data and 4x4 reduces bit rate >16x.
  - Example 2: Digital film emulation
    - Digitally develop "grain"
  - Example 3: Codebook compression
  - Example 4: Implement compressive sensing*
    - Transform to compressed frame $\underline{y}$ where
    - $\underline{y} = \underline{A}\ \underline{f}$ where $\underline{A}$ is m x n random Bernoulli matrix and $\underline{f}$ is (sparse) vectorized binary bit plane of n elements (23Gb).
    - Data rate reduction factor is n/m.

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QUANTA
IMAGE
SENSOR
(QIS)

ON-CHIP
PROCESSOR
PROGRAM

ROW DRIVERS

JOT ARRAY

READ POINTER

RESET POINTER

APERTURE

BIT PLANE
DATA

TIMING AND CONTROL

COLUMN SENSE AMPLIFIERS

ACCUMULATING LOGIC+MEMORY

KERNEL PROCESSOR

OUTPUT MULTIPLEXER

n x n AGGREGATION

OFF CHIP MEMORY +
IMAGE FORMATION PROCESSOR

TEMPORAL
AGGREGATION

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- IDEALISM: Counting photon strikes "without" read noise is nearly ideal. (Measuring energy would be even better.) Photon counting keeps quantized light in the quantized (bit) domain

- ALIGNMENT: Future nanoelectronics (e.g. graphene technology) may not allow integration of photocarriers within the semiconductor.

- TIMING: Soon, mainstream microelectronics technology will enable realization of a QIS.

- IMAGING PERFORMANCE:

  - QIS puts most analog signal processing into the digital domain at the earliest opportunity taking advantage of improvements and the flexibility of digital signal processing.

  - Improved low light imaging.

  - Improved tracking of targets in space and time

  - TDI in any scan direction

  - Time-resolved scientific low-light imaging with high resolution

  - Emulation of different image formation processes easily achieved, such as "digital film"

- Application studies
- Architectural studies
- Development of jot device(s)
- Signal chain
- On-chip kernel processor
- Off-chip image formation algorithms
- Power management
- Noise shaping and other digital signal processing algorithms.
- End to end system simulation
- Work started in several areas at Dartmouth

- Quanta Image Sensor (QIS) "vision" is to count every photon that hits the sensor, recording its location and arrival time, and create pixels from bit-planes of data
- QIS driven by at least four factors
    - Pixel shrink runs into full well capacity issues.
    - Optical resolution limited by diffraction limit
    - Strong drive to sub-electron read noise
    - Future CMOS processes may not be well aligned to CMOS APS needs and trends.
- QIS is a paradigm shift in the way we do imaging
- Too early to tell if this will have a compelling advantage for consumer electronics, but looks promising for scientific and aerospace apps.
- We are at the beginning.