Second generation solid-state image sensor technology
Retains nearly all the performance of a CCD
Unique advantages of CMOS APS:
  – Ultra low power system, >100x less than CCD system
  – Highly integrated on-chip electronics reduces component count
  – Commercial CMOS technology leverage
  – Don’t need a dedicated CCD fab line to make sensors ($$)
  – Random access and window-of-interest pixel readout
  – Standard 5 volt (or 3.3 volt) operation
  – Faster readout
  – Radiation hard
  – Larger format arrays
Strong commercial, biomedical, defense, and space applications
PROBLEMS WITH CCDs

• Charge-coupled devices (CCDs) invented around 1970.
  – Uses repeated lateral charge transfer to readout image.
• Need for nearly perfect charge transfer efficiency is Achilles’ heel.
  – Requires specialized fabrication process so not 100% CMOS compatible.
  – Requires numerous different voltages to achieve good performance
  – Susceptible to bulk radiation damage so radiation “soft”
• CCDs are large capacitance devices so on-chip drive circuits difficult to implement.
  – Excessive power dissipation
  – Hot electron photon emission
  – Process incompatibility
• On-chip signal processing (e.g. ADC) difficult to implement in CCD technology.
EVOLUTION OF MICROELECTRONICS
FEATURE SIZE

Enough space to put amplifier into each pixel.
RESOLUTION LIMITS

Airy Disk Diameter
\[ D = 2.44 \lambda F# \]

Cheap Lens Resolution
(30 lp/mm)

High Performance Lens Resolution
(120 lp/mm)
COMMON CMOS PIXELS

Passive Pixel
- 1 transistor pixel
- 10 L scaling
- Great QE
- Poor noise (250 e-)
- Poor large & fast scaling

Photodiode CMOS APS
- 3 transistor pixel
- 15 L scaling
- Great QE
- OK noise (50-100 e-)
- Good large & fast scaling

Photogate CMOS APS
- 5 transistor pixel
- 20 L scaling
- Good QE
- Great noise (15 e-)
- Good large & fast scaling
28x28
cc256
FOTOS
SXRS
JPL AT&T Digital QCIF
AT&T 10 um CIF
JPL AT&T 1Kx1K
APS and CCD Measured Quantum Efficiencies

Wavelength (nm)

Quantum Efficiency

N5 APS
N2 APS
P1 APS
Cassini CCD
AT&T APS
cc128
TI VP (FF)
KAI-0370
FT8
SCALING TREND IN CMOS APS

Pixel Size (microns) vs. Drawn Design Rule (L)

- 20L
- 15L
- 10L

- JPL
- AT&T/JPL
- NHK
<table>
<thead>
<tr>
<th>PRINCIPAL DEVICE TECHNOLOGY CHARACTERISTICS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum lithographic feature size (0.7x/gen) [μm]</td>
</tr>
<tr>
<td>Isolation</td>
</tr>
<tr>
<td>Gate Oxide [nm]</td>
</tr>
<tr>
<td>Gate Electrode</td>
</tr>
<tr>
<td>Substrate doping [cm⁻³]</td>
</tr>
<tr>
<td>Source/drain junction</td>
</tr>
<tr>
<td>Source/drain junction depth [μm]</td>
</tr>
<tr>
<td>Power supply [V]</td>
</tr>
<tr>
<td>Threshold voltage [V]</td>
</tr>
<tr>
<td>Threshold voltage variation [+/- mV, wafer-wafer]</td>
</tr>
<tr>
<td>DRAM bits/chip (4x/generation)</td>
</tr>
<tr>
<td>DRAM chip size (1.5x/generation) [mm²]</td>
</tr>
<tr>
<td>DRAM cell size (0.4x/generation) [μm²]</td>
</tr>
<tr>
<td>SRAM bits/chip (4x/generation)</td>
</tr>
<tr>
<td>SRAM chip size (1.5x/generation) [mm²]</td>
</tr>
<tr>
<td>SRAM cell size (0.4x/generation) [μm²]</td>
</tr>
<tr>
<td>CMOS APS pixel pitch (0.7x/generation, 20L) [μm]</td>
</tr>
<tr>
<td>CMOS APS image pixel size (0.5x/generation, 20L) [μm²]</td>
</tr>
<tr>
<td>CMOS APS fill factor</td>
</tr>
<tr>
<td>Imager format size (HDTV)</td>
</tr>
<tr>
<td>Imager format size (NTSC-TV)</td>
</tr>
</tbody>
</table>
Silicide (polycide/salicide)

- Opaque layer used to reduce resistivity of poly and S/D junctions
- CoSi$_2$ less opaque than TiSi$_2$
- Used below $L < 0.8 - 0.35$ microns
- Mask for removal “not a big deal” (std. layer in some processes)
- Not used in DRAM processes
- Possibly useful as additional light shield

Fill factor

- Smaller $L$ yields larger fill factor for given pixel pitch
Carrier Collection Depth
- Depletion region shrinking
  - lower operating voltage
  - higher substrate doping concentrations
- Loss at p+ substrate/p-epi interface due to gettering at interface
- SOI thickness < 200 nm
- Retrograde wells retards collection from neutral region (built-in field)

Thinner Polysilicon
- 1.5 - 2.0 micron process, poly typically 400 nm thickness
- 0.5 micron process poly -> 200 nm thickness
CONSEQUENCES OF TECHNOLOGY SCALING

CROSSTALK

Isolation
• LOCOS --> Shallow Trench Isolation (STI)
  – not much effect - may actually be improvement:
  – less stress
  – more radiation hard
  – less dark current
• Deep trench possible (DRAM-like process)
• SOI eliminates all crosstalk (and most QE)

Shallower depletion regions
• Tend to increase longer wavelength crosstalk since more diffusion

Upper metal layers yield loose light shields
CONSEQUENCES OF TECHNOLOGY SCALING

DARK CURRENT

- “OFF” Currents increase
  - shorter length
  - lower threshold voltage
- Higher doping will increase pn junction leakage currents
- Better contamination control will lower dark current
- Gate oxide tunneling current not too important
  - current scales with electric field (i.e. signal charge)
  - tunneling current looks mostly like majority carrier current
  - minority carrier tunneling will lead to “anti-blooming effect”
- Gate-induced leakage current a concern in higher doped junctions
- Hot carrier effects not expected to increase due to voltage scaling
DYNAMIC RANGE

- Define as ratio of saturation signal to noise floor
- Transistor noise
  - $1/f$ noise, white noise increases for smaller area
  - noise reduces for lower voltages
- Reduced capacitances will increase conversion gain ($\mu V/e^-$)
- Reduced operating voltage will decrease saturation signal
- Reduced threshold voltages will increase saturation signal
- Well capacity of PG devices increase with decreased gate oxide thickness
- Net effect may result in constant dynamic range
READOUT SPEED

- Dominated by parasitic capacitances and transistor sizing
- Wiring capacitance per unit length remains about constant
- Smaller pixel size, same no. elements, speed increases

DIE SIZE / ARRAY SIZE

- DRAM trend will drive toward larger die sizes
- Array size can increase like DRAM trend
- 17 - 20 mm standard (4Kx4K for 5 micron pixel)
- Larger tools will become available (e.g. 48 mm Canon tool)
- CMOS APS amenable to e-beam wafer scale integration
- CMOS APS amenable to stitching strategies for wafer scale integration
CONSEQUENCES OF TECHNOLOGY SCALING

SUMMARY

QUANTUM EFFICIENCY: Looks OK until SOI

CROSSTALK: Increases but no show stopper

DARK CURRENT: Some increase possible

DYNAMIC RANGE: Should remain nearly constant

READOUT SPEED: Faster readout for fixed array size

DIE SIZE/ARRAY SIZE: Smaller die for fixed array size
Larger arrays possible
COMPETITIVE CCDs

Expect increased competition from CCDs:

- Reduced parasitic capacitances --> lower power
- Lower voltage operation
- Higher fill factor using smaller design rules
- Increasing use of CMOS/CCD combined process
  - On-chip timing and control
  - On-chip drivers using BiCMOS (?)
  - On-chip signal chain, ADC
- Reduced cost for Mpixel sensors
## APS VS. CCD

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>APS</th>
<th>CCD</th>
</tr>
</thead>
<tbody>
<tr>
<td>FORMAT</td>
<td>Wafer scale (8”)</td>
<td>8096x8096 (2”)</td>
</tr>
<tr>
<td>VOLTAGE</td>
<td>3.3 VOLTS</td>
<td>+/-20.0 VOLTS</td>
</tr>
<tr>
<td>SYS. POWER</td>
<td>0.05 W</td>
<td>5 W</td>
</tr>
<tr>
<td>ON-CHIP TIMING</td>
<td>yes</td>
<td>none</td>
</tr>
<tr>
<td>WINDOW READOUT</td>
<td>yes</td>
<td>none</td>
</tr>
<tr>
<td>ON CHIP ADC RES.</td>
<td>10-12 bits</td>
<td>none</td>
</tr>
<tr>
<td>PIXEL SIZE</td>
<td>5 micron</td>
<td>5 micron</td>
</tr>
<tr>
<td>PROCESS</td>
<td>0.25 um CMOS</td>
<td>0.6 um CCD</td>
</tr>
<tr>
<td>FILL FACTOR</td>
<td>25%</td>
<td>25%</td>
</tr>
<tr>
<td>CONVERSION GAIN</td>
<td>10 uV/e-</td>
<td>10 uV/e-</td>
</tr>
<tr>
<td>SATURATION</td>
<td>100,000 e-</td>
<td>50,000 e-</td>
</tr>
<tr>
<td>INPUT REF. NOISE</td>
<td>15 e-</td>
<td>10 e-</td>
</tr>
<tr>
<td>DYNAMIC RANGE</td>
<td>74 dB</td>
<td>75 dB</td>
</tr>
<tr>
<td>PEAK QE</td>
<td>30%</td>
<td>25%</td>
</tr>
</tbody>
</table>
DISCUSSION

CCDs

CMOS APS

Mainstream CMOS Technology

System Miniaturization Cost


Window of Opportunity