ACTIVE PIXEL SENSORS VS. CHARGE-COUPLED DEVICES

Dr. Eric R. Fossum

Imaging Systems Section
Jet Propulsion Laboratory, California Institute of Technology
(818) 354-3128

1993 IEEE Workshop on CCDs and Advanced Image Sensors
OUTLINE

1. A Brief History of CCDs
2. Active Pixel Sensors
3. State of the Art
4. Comparison of APS vs. CCD Technology
5. Speculation
6. Summary
EVOLUTION OF

PHOTOLITHOGRAPHIC FEATURE SIZE VS. PIXEL SIZE

<table>
<thead>
<tr>
<th>YEAR</th>
<th>DIMENSION (microns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1970</td>
<td>100</td>
</tr>
<tr>
<td>1975</td>
<td>10</td>
</tr>
<tr>
<td>1980</td>
<td>1</td>
</tr>
<tr>
<td>1985</td>
<td>0.1</td>
</tr>
<tr>
<td>1990</td>
<td></td>
</tr>
<tr>
<td>1995</td>
<td></td>
</tr>
<tr>
<td>2000</td>
<td></td>
</tr>
</tbody>
</table>

CCD Invented
Typ. Diffraction Limit
Design Rule

Pixel Size
## TYPICAL CCD PERFORMANCE

<table>
<thead>
<tr>
<th></th>
<th>COMMERCIAL</th>
<th>SCIENTIFIC</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Array Size</strong></td>
<td>1920x1036</td>
<td>2048x2048</td>
</tr>
<tr>
<td><strong>CTE</strong></td>
<td>&gt;0.99997</td>
<td>&gt;0.999995</td>
</tr>
<tr>
<td><strong>Architecture</strong></td>
<td>FIT 1&quot;</td>
<td>Full Frame</td>
</tr>
<tr>
<td><strong>Smear</strong></td>
<td>-110 dB</td>
<td>n/a</td>
</tr>
<tr>
<td><strong>Full Well</strong></td>
<td>120,000</td>
<td>40,000</td>
</tr>
<tr>
<td><strong>Noise</strong></td>
<td>20-30 e-</td>
<td>3-5 e-</td>
</tr>
<tr>
<td><strong>Dynamic Range</strong></td>
<td>75 dB</td>
<td>80 dB</td>
</tr>
<tr>
<td><strong>Power Dissipation</strong></td>
<td>1.5 W</td>
<td>&lt;10 mW</td>
</tr>
<tr>
<td><strong>Pixel Size</strong></td>
<td>7.3 µm x 7.6 µm</td>
<td>7.5 µm x 7.5 µm</td>
</tr>
<tr>
<td><strong>Aperture</strong></td>
<td>&gt;60% with microlens</td>
<td>&gt;90 %</td>
</tr>
</tbody>
</table>
ADVANTAGES OF CCDS

- Incumbent technology
- Large formats demonstrated
- Very small pixels possible
- Noiseless charge domain processing (e.g. binning, TDI)
SOME RELEVANT PROBLEMS WITH CCDS

1. Need for nearly perfect charge transfer efficiency
   - Signal fidelity \( \sim \eta^m \), \( \eta = \text{CTE}, m = \# \text{ of stages} \)
   - e.g. \( \eta = 0.99995, m = 8000 \), yields fidelity of 0.67

2. Radiation softness
   - Particularly susceptible to bulk silicon damage (reduced CTE)

3. Susceptible to smear
   - Requires good light shield, FIT structure

4. High power dissipation on-chip for large, fast arrays
   - Large capacitances to drive
   - Large voltage swings (power \( \sim CV^2f \), electroluminescence)
5. Difficult to integrate on-chip electronics
   - Requires high power drive electronics
   - Many voltages required
   - Process incompatible for practical CMOS signal chain integration

6. Difficult to extend spectral range
   - Want UV response $\lambda < 0.4$ microns
   - Want SWIR response to 2.5 microns
   - High CTE in non-silicon materials unlikely
   - Backside illumination fraught with problems

7. Limited readout rate
   - HDTV rates (70 MHz) require dual channel architecture
OTHER SOLID-STATE IMAGER TECHNOLOGIES

PHOTODIODE ARRAYS

- High noise (>250 e- r.m.s.)
- Lag
- Good blue/UV response

CIDS

- High noise (~ 200 e- r.m.s.)
- Non-destructive readout

HYBRID IR FPAs

- High fill factor
- Medium noise (30-50 e- r.m.s.)
- Hybrids expensive, small array sizes (<512x512)

ACTIVE PIXEL SENSOR CONCEPT
One or more active transistors in the pixel.

- Eliminates the need for charge transfer
- Buffer the output signal
- Provides high sensitivity (low C)
- Provides current drive capability
- Provides random access capability
- Allows low power readout
- Simplifies system design
(insert George VG here)
JPL CMOS ACTIVE PIXEL SENSOR

First Silicon Demonstrated:

- 100% TTL compatible input (0.5 V) on all input signals.
- X-Y addressability.
- Differential analog output signal.
- Lateral antiblooming control.
- Low read noise (22 e- rms expected)
- High sensitivity (4 μV/e-)
- Low dark current (1-10 nA/cm²)
- High dynamic range (600 mV saturation)
- Low fixed pattern noise (<1.5% saturation)
- Vanilla CMOS design.
MICROLENS ARRAY TO INCREASE EFFECTIVE FILL FACTOR

hv

"Dead" region

Photosensitive region
## SUMMARY OF STATE OF THE ART

<table>
<thead>
<tr>
<th>Developer</th>
<th>DGFSPT</th>
<th>CMD</th>
<th>BCMD</th>
<th>BASIS</th>
<th>SIT</th>
<th>AMI</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toshiba</td>
<td>Olympus</td>
<td>Texas Instr.</td>
<td>Canon</td>
<td>Olympus</td>
<td>NHK</td>
<td>JPL/Caltech</td>
<td></td>
</tr>
<tr>
<td>APS Type</td>
<td>Lateral</td>
<td>Vertical</td>
<td>Vertical</td>
<td>Vertical</td>
<td>Lateral</td>
<td>Lateral</td>
<td>Lateral</td>
</tr>
<tr>
<td>Output</td>
<td>Lateral</td>
<td>Lateral</td>
<td>Lateral</td>
<td>Vertical</td>
<td>Lateral</td>
<td>Lateral</td>
<td>Lateral</td>
</tr>
<tr>
<td>Pixel Size (μm)</td>
<td>13 x 13</td>
<td>5.0 x 5.2</td>
<td>10 x 10*</td>
<td>13.5 x 13.5</td>
<td>17 x 13.5</td>
<td>17.3x13.5</td>
<td>40 x 40*</td>
</tr>
<tr>
<td>Sensitivity</td>
<td>200 μV/e-</td>
<td>965 pA/e+</td>
<td>15.4 μV/e-</td>
<td>3.5 μV/e+</td>
<td>3.0 μV/e+</td>
<td>1.6 μV/e-</td>
<td>4.0 μV/e-</td>
</tr>
<tr>
<td>Input-Noise</td>
<td>0.8 e- rms</td>
<td>11.2 e+ rms</td>
<td>15 e- rms</td>
<td>60 e+ rms</td>
<td>69 e+ rms</td>
<td>130 e- rms*</td>
<td>22 e- rms</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td>75 dB</td>
<td>68 dB</td>
<td>72 dB</td>
<td>76 dB</td>
<td>86.5 dB</td>
<td>77 dB</td>
<td>82 dB</td>
</tr>
<tr>
<td>FPN (p-p)</td>
<td>10 %</td>
<td>6 %</td>
<td>2 %</td>
<td>0.03 %</td>
<td>1.1 %</td>
<td>0.2 %</td>
<td>1.5 %</td>
</tr>
<tr>
<td>Anti-blooming</td>
<td>vertical</td>
<td>vertical*</td>
<td>vertical</td>
<td>none*</td>
<td>none*</td>
<td>lateral</td>
<td>lateral</td>
</tr>
<tr>
<td>Lag</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>&lt;0.1 %</td>
<td>70 %</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Note</td>
<td>discont.</td>
<td>*uses horiz. blnk.</td>
<td>*hex. layout</td>
<td>*uses clipping op</td>
<td>discont.</td>
<td>*100x gain e-beam=1.3</td>
<td>*2 μm design rule</td>
</tr>
</tbody>
</table>
STATE OF THE ART:

TOSHIBA DOUBLE-GATE FLOATING SURFACE TRANSISTOR

- sensitivity of 200 μV/e-
- read noise 0.8 e- rms
- needs large voltage on DG
STATE OF THE ART:
OLYMPUS CHARGE-MODULATION DEVICE (CMD)

- small pixel (5.0 μm x 5.2 μm)
- gain is 965 pA/hole, 11.2 e+ rms noise
- readout is current mode
- dark current and FPN problem
STATE OF THE ART:
TI BULK CHARGE-MODULATED DEVICE (BCMD)

- sensitivity 15 $\mu$V/e-
- read noise 15 e- r.m.s.
- complex vertical layer structure
STATE OF THE ART

CANON BASE-STORED IMAGE SENSOR (BASIS)

- sensitivity 3.5 $\mu$V/e+, but kTC noise
- very low FPN (0.03%)
- good fill factor, blue response
STATE OF THE ART:
OLYMPUS STATIC INDUCTION TRANSISTOR

- sensitivity 3.0 μV/e+
- large dynamic range
- large lag problem
STATE OF THE ART

NHK AMPLIFIED MOS IMAGER (AMI)

- 100 x gain due to avalanche effect in a-Si
- 130 e- kTC noise = 1.3 e- photocathode-referred noise
- photocathode QE = 10 %
## COMPARISON OF APS TECHNOLOGIES

<table>
<thead>
<tr>
<th>Feature</th>
<th>DGFSPT</th>
<th>CMD</th>
<th>BCMD</th>
<th>BASIS</th>
<th>SIT</th>
<th>AMI</th>
<th>CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPN</td>
<td>x</td>
<td>x</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Random Noise</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Small Pixel</td>
<td>x</td>
<td>✓</td>
<td>✓</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Fill Factor</td>
<td></td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>x</td>
</tr>
<tr>
<td>Voltages</td>
<td></td>
<td>x</td>
<td>✓</td>
<td></td>
<td></td>
<td>x</td>
<td>✓</td>
</tr>
<tr>
<td>Microlens</td>
<td>✓</td>
<td>x</td>
<td>x</td>
<td>✓</td>
<td>x</td>
<td>x</td>
<td>✓</td>
</tr>
<tr>
<td>Snapshot (Transfer)</td>
<td>✓</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>✓</td>
</tr>
<tr>
<td>CMOS Integration</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

E.R.Fossum 1/1/2008 CANADA pg. 20
## APS VS. CCD

<table>
<thead>
<tr>
<th>Major Strengths</th>
<th>APS</th>
<th>CCD</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Low Power</td>
<td>Incumbent Technology</td>
</tr>
<tr>
<td></td>
<td>On-Chip Integration</td>
<td>Small Pixels</td>
</tr>
<tr>
<td></td>
<td>Low Smear</td>
<td>5k x 5k Demo'd</td>
</tr>
<tr>
<td></td>
<td>Radiation Hardness</td>
<td>Charge-domain processing</td>
</tr>
<tr>
<td></td>
<td>Random Access</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Major Weaknesses</th>
<th>Lower Fill-Factor</th>
<th>Power Requirements</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>FPN Susceptibility</td>
<td>Incompatible w/ Integratn</td>
</tr>
<tr>
<td></td>
<td>Newer Technology</td>
<td>Need for perfect CTE</td>
</tr>
</tbody>
</table>

E.R. Fossum  1/1/2008 CANADA pg. 21
SPECULATION

- Smart Sensors
- Machine Vision
- Linear Arrays
- Consumer Video
- Consumer Still
- Broadcast Video
- Scientific Mini cameras
- Scientific Imaging

Legend:
- = CCD
- = APS
SUMMARY

• Active pixel sensors are a new, emerging technology

• APS is already becoming competitive to CCDs

• The major strength of CCDs is incumbency and current state of the art in IC design rules.

• APS needs to improve FPN using improved fab. and on-chip signal processing.

• APS is a stepping stone to highly integrated opto-electronic sensor systems (e.g. a camera on a chip)

• CCDs are future "dinosaurs".
ACKNOWLEDGMENTS

S. Mendis, Columbia University
R. Gee, S. Kemeny, B. Pain, C. Stevens, V. Sarohia, JPL
G. Johnston, W. Hudson, NASA HQ
Discussions with Kodak, Polaroid, Orbit,
Olympus, NEC, NHK, Sony, Toshiba, Canon, Matsushita,
Philips, Texas Instruments

The research described in this paper was carried out by the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.